

## 13A, 500V N-CHANNEL MOSFET

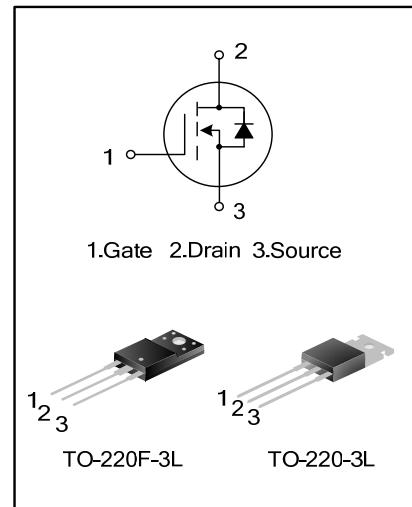
### GENERAL DESCRIPTION

SVD13N50T/F is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary S-Rin™ structure DMOS technology. The improved planar stripe cell and the improved guarding ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.

### FEATURES

- \* 13A,500V,R<sub>Ds(on)</sub>(typ)=0.36Ω@V<sub>GS</sub>=10V
- \* Low gate charge
- \* Low C<sub>rss</sub>
- \* Fast switching
- \* Improved dv/dt capability



### ORDERING SPECIFICATIONS

Part No.	Package	Marking	Material	Packing
SVD13N50T	TO-220-3L	SVD13N50T	Pb free	Tube
SVD13N50F	TO-220F-3L	SVD13N50F	Pb free	Tube

### ABSOLUTE MAXIMUM RATINGS (T<sub>c</sub>=25°C unless otherwise noted)

Parameter	Symbol	Rating		Unit
		SVD13N50T	SVD13N50F	
Drain-Source Voltage	V <sub>DS</sub>	500		V
Gate-Source Voltage	V <sub>GS</sub>	±30		V
Drain Current	I <sub>D</sub>	13		A
Power Dissipation(T <sub>c</sub> =25°C)	P <sub>D</sub>	180	51	W
Single Pulsed Avalanche Energy (Note 1)	E <sub>AS</sub>	1446		mJ
Operation Junction Temperature	T <sub>J</sub>	150		°C
Storage Temperature	T <sub>STG</sub>	-55~+150		°C

**THERMAL CHARACTERISTICS**

Parameter	Symbol	Rating		Unit
		SVD13N50T	SVD13N50F	
Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	1.25	5	°C/W
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	62.5	120	°C/W

**ELECTRICAL CHARACTERISTICS (T<sub>c</sub>=25°C unless otherwise noted)**

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B <sub>VDSS</sub>	V <sub>Gs</sub> =0V, I <sub>D</sub> =250μA	500	--	--	V
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>Ds</sub> =650V, V <sub>Gs</sub> =0V	--	--	1	μA
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>Gs</sub> =±30V, V <sub>Ds</sub> =0V	--	--	±100	nA
Gate Threshold Voltage	V <sub>Gs(th)</sub>	V <sub>Gs</sub> = V <sub>Ds</sub> , I <sub>D</sub> =250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	R <sub>Ds(on)</sub>	V <sub>Gs</sub> =10V, I <sub>D</sub> =6.5A	--	0.36	0.52	Ω
Input Capacitance	C <sub>iss</sub>	V <sub>Ds</sub> =25V, V <sub>Gs</sub> =0V, f=1.0MHZ	--	1838	--	pF
Output Capacitance	C <sub>oss</sub>		--	194	--	
Reverse Transfer Capacitance	C <sub>rss</sub>		--	10.6	--	
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =250V, I <sub>D</sub> =6.5A, R <sub>G</sub> =4.7Ω, V <sub>Gs</sub> =10V (Note 2,3)	--	52	--	ns
Turn-on Rise Time	t <sub>r</sub>		--	40	--	
Turn-off Delay Time	t <sub>d(off)</sub>		--	352	--	
Turn-off Fall Time	t <sub>f</sub>		--	40	--	
Total Gate Charge	Q <sub>g</sub>	V <sub>Ds</sub> =400V, I <sub>D</sub> =13A, V <sub>Gs</sub> =10V (Note 2,3)	--	53.18	--	nC
Gate-Source Charge	Q <sub>gs</sub>		--	11.08	--	
Gate-Drain Charge	Q <sub>gd</sub>		--	17.17	--	

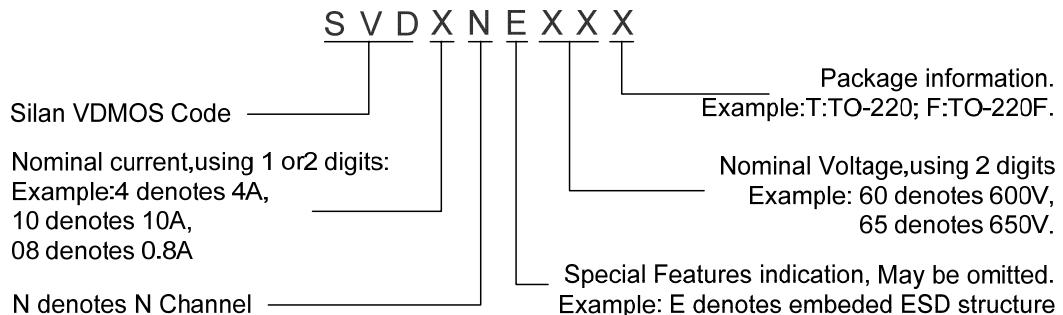
**SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS**

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I <sub>S</sub>	Integral Reverse p-n Junction Diode in the MOSFET	--	--	13	A
Pulsed Source Current	I <sub>SM</sub>		--	--	52	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =13A, V <sub>Gs</sub> =0V	--	--	1.4	V
Reverse Recovery Time	T <sub>rr</sub>	I <sub>S</sub> =13A, V <sub>Gs</sub> =0V, dI/dt=100A/μS (Note 2)	--	450	--	ns
Reverse Recovery Charge	Q <sub>rr</sub>		--	5.0	--	μC

Notes:

1. L=30mH, I<sub>AS</sub>=7.725A, V<sub>DD</sub>=250V, R<sub>G</sub>=25Ω, starting T<sub>J</sub>=25°C;
2. Pulse Test: Pulse width ≤300μs, Duty cycle≤2%;
3. Essentially independent of operating temperature.

## NOMENCLATURE



## TYPICAL CHARACTERISTICS

Figure 1. On-region characteristics

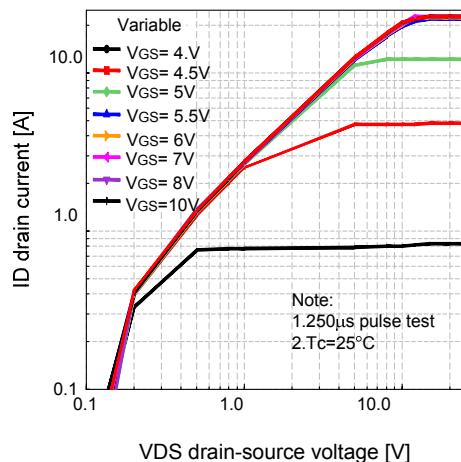


Figure 2. Transfer characteristics

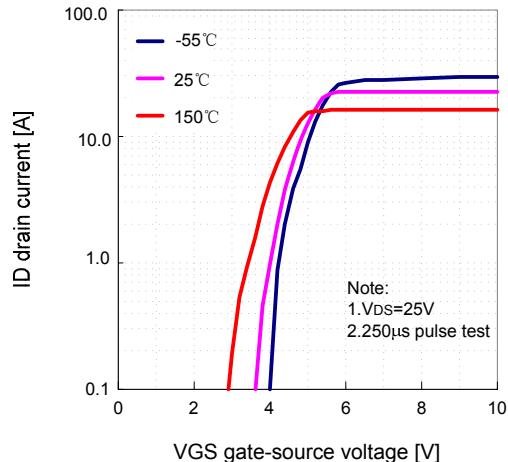


Figure 3. On-resistance variation vs. drain current and gate voltage

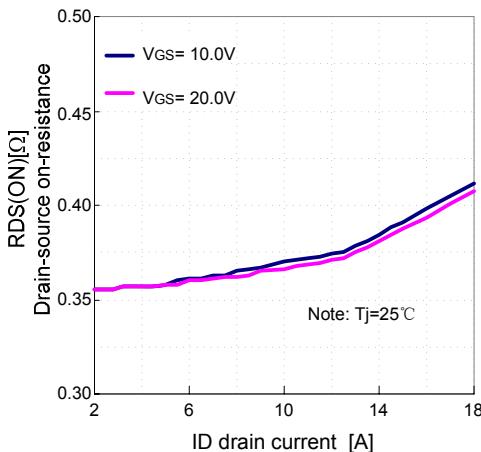
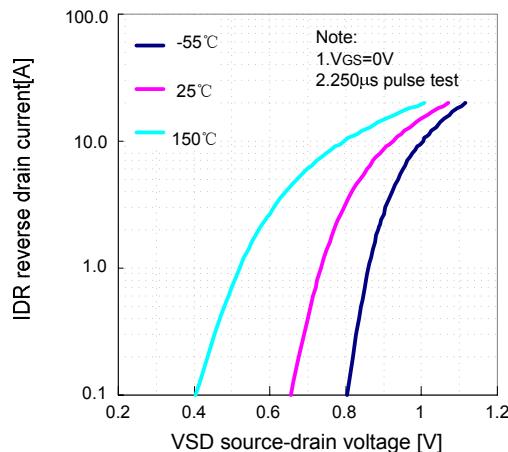


Figure 4. Body diode forward voltage variation vs. source current



## TYPICAL CHARACTERISTICS(continued)

Figure 5. capacitance characteristics

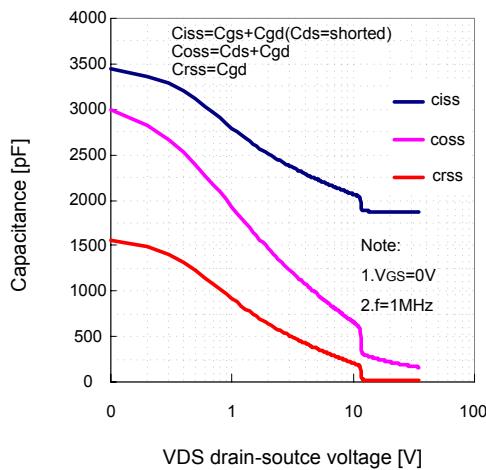


Figure 6. gate charge characteristics

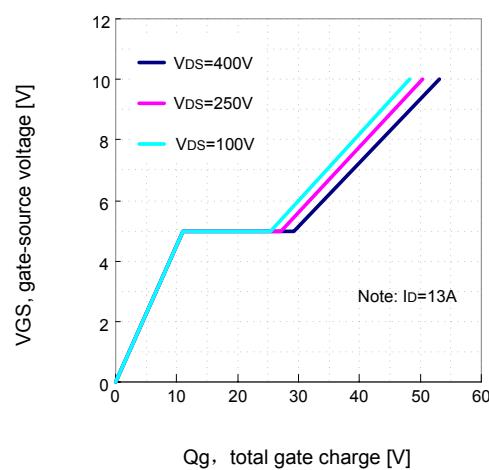


Figure 7. breakdown voltage variation vs. temperature

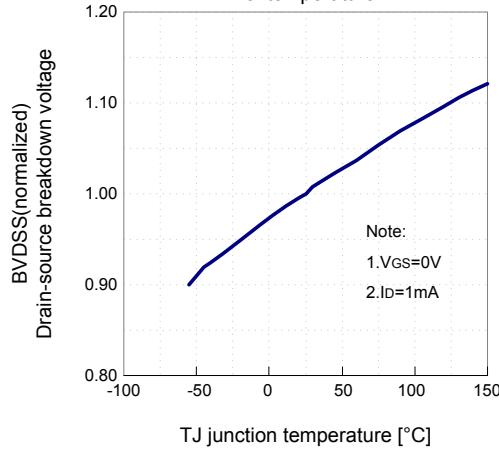
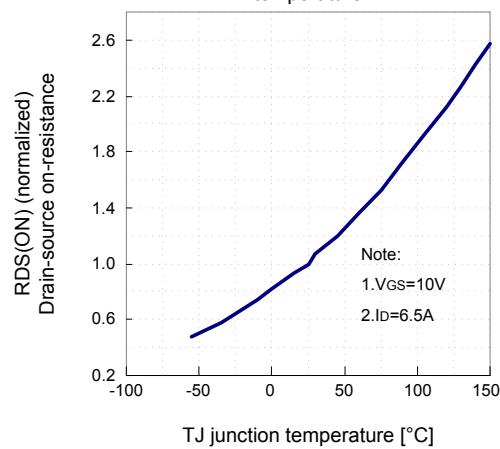
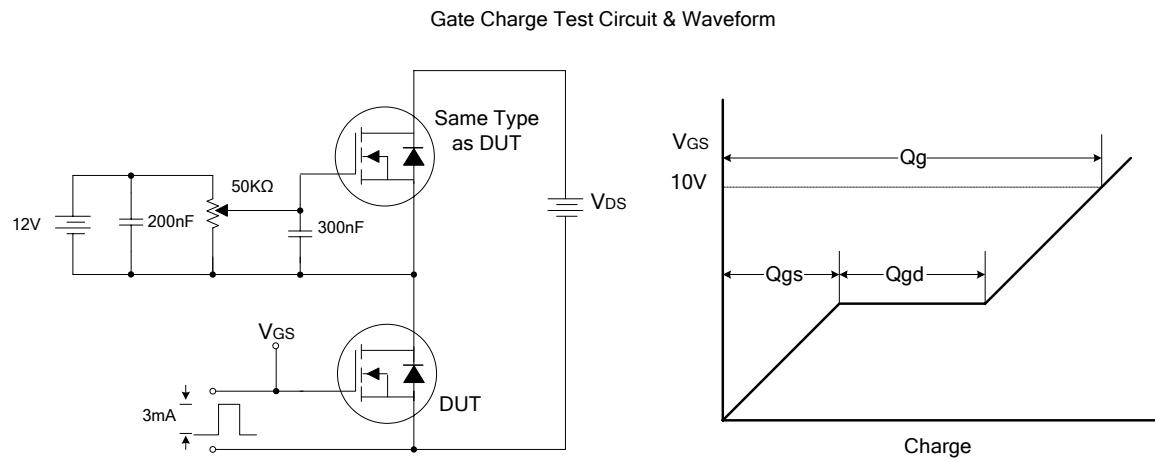


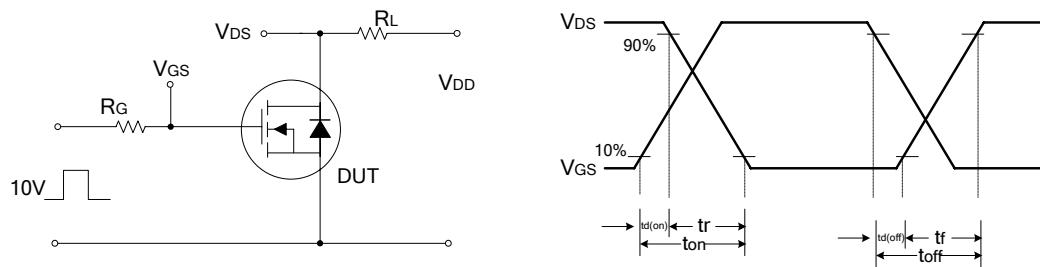
Figure 8. on-resistance variation vs. temperature



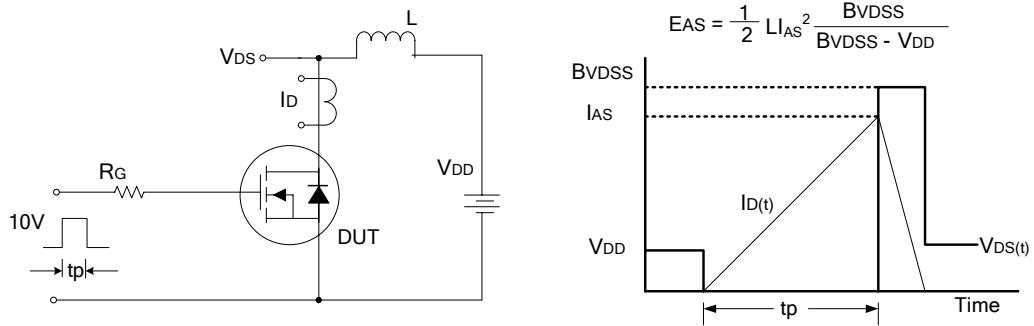
## TYPICAL TEST CIRCUIT



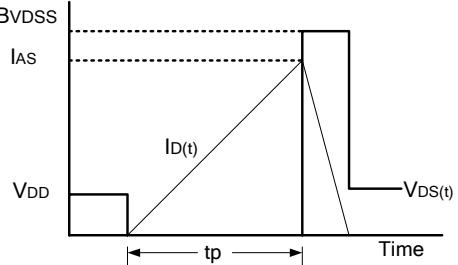
## Resistive Switching Test Circuit & Waveform



## Unclamped Inductive Switching Test Circuit & Waveform



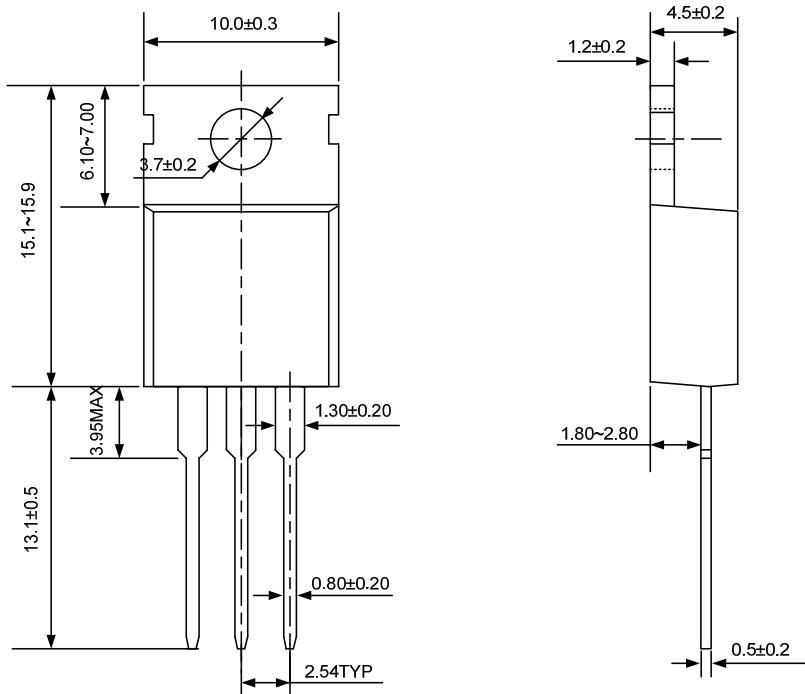
$$EAS = \frac{1}{2} L I_{AS}^2 \frac{BVDSS}{BVDSS - VDD}$$



## PACKAGE OUTLINE

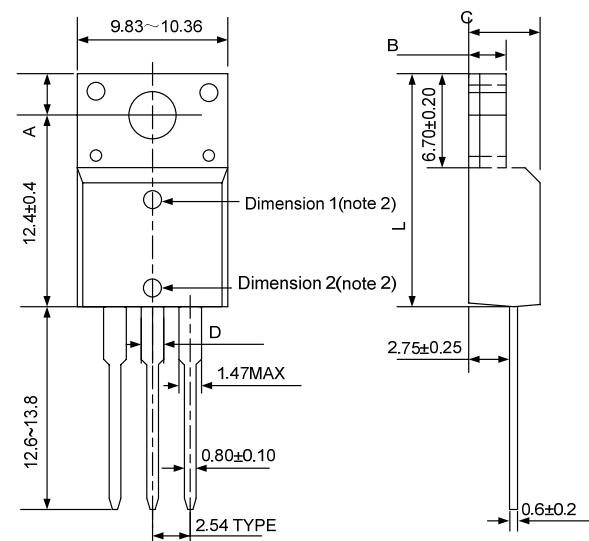
**TO-220-3L**

**UNIT: mm**



**TO-220F-3L**

**UNIT: mm**



Symbol(note1)	Dimension1	Dimension2
A	3.30±0.15	2.70±0.15
B	2.55±0.20	3.0±0.20
C	4.72±0.2	4.50±0.20
D	1.47MAX	1.75MAX
L	15.75±0.30	15.00±0.30

Note1: There may be two values for some products due to different plastic mould machine, so two dimensions of the same position are listed;

Note2: When the product size is Dimension1, the thimble hole is on top of the surface; when the size is Dimension2, the center hole is on bottom of the surface.

**Disclaimer:**

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- All semiconductor products malfunction or fail with some probability under special conditions. When using Silan products in system design or complete machine manufacturing, it is the responsibility of the buyer to comply with the safety standards strictly and take essential measures to avoid situations in which a malfunction or failure of such Silan products could cause loss of body injury or damage to property.
- Silan will supply the best possible product for customers!

## ATTACHMENT

## Revision History

Date	REV	Description	Page
2010.05.14	1.0	Original	
2010.10.21	1.1	Modify "ORDERING SPECIFICATIONS", the parameters, the template of Datasheet	