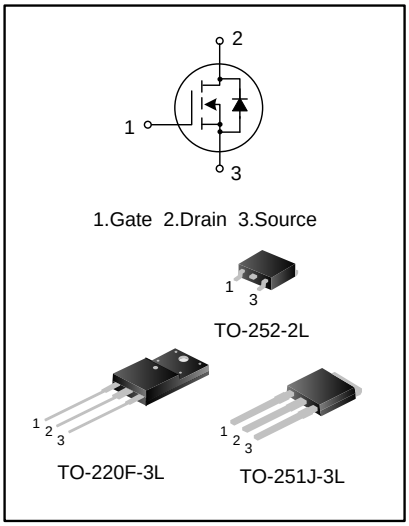
7A, 650V DP MOS POWER TRANSISTOR

GENERAL DESCRIPTION

SVS7N65F/D/MJ is an N-channel enhancement mode high voltage power MOSFETs produced using the new platform of Silan's DP MOS technology. It achieves low conduction loss and switching losses. It leads the design engineers to their power converters with high efficiency, high power density, and superior thermal behavior. Furthermore, it's universal applicable, i.e., suitable for hard and soft switching topologies.



FEATURES

- 7A, 650V, $R_{DS(on)(typ)}$=0.66Ω@V_{GS}=10V
- New revolutionary high voltage technology
- Ultra low gate charge
- Periodic avalanche rated
- Extreme dv/dt rated
- High peak current capability

ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SVS7N65F	TO-220F-3L	SVS7N65F	Halogen free	Tube
SVS7N65D	TO-252-2L	SVS7N65D	Halogen free	Tube
SVS7N65DTR	TO-252-2L	SVS7N65D	Halogen free	Tape & Reel
SVS7N65MJ	TO-251J-3L	SVS7N65MJ	Halogen free	Tube

ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Characteristics		Symbol	Ratings			Unit
			SVS7N65F	SVS7N65D	SVS7N65MJ	
Drain-Source Voltage		V_{DS}	650			V
Gate-Source Voltage		V_{GS}	±30			V
Drain Current	T_C=25°C	I_D	7.0			A
	T_C=100°C		4			
Drain Current Pulsed		I_{DM}	25			A
Power Dissipation(T_C=25°C)		P_D	35	48	50	W
-Derate above 25°C			0.28	0.38	0.40	W/°C
Single Pulsed Avalanche Energy (Note 1)		E_{AS}	263			mJ
Operation Junction Temperature Range		T_J	-55～+150			°C
Storage Temperature Range		T_{stg}	-55～+150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings			Unit
		SVS7N65F	SVS7N65D	SVS7N65MJ	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3.57	2.60	2.50	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	120	110	110	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B_{VDSS}	V_{GS}=0V, I_D=250μA	650	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=650V, V_{GS}=0V	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=3.5A	--	0.66	0.77	Ω
Input Capacitance	C_{iss}	V_{DS}=100V, V_{GS}=0V, f=1.0MHz	--	486	--	pF
Output Capacitance	C_{oss}		--	30.5	--	
Reverse Transfer Capacitance	C_{rss}		--	2.8	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=325V, I_D=7.0A, V_{GS}=10V, R_G=10Ω (Note 2,3)	--	11.0	--	ns
Turn-on Rise Time	t_r		--	28.6	--	
Turn-off Delay Time	$t_{d(off)}$		--	45.2	--	
Turn-off Fall Time	t_f		--	29.1	--	
Total Gate Charge	Q_g	V_{DS}=520V, I_D=7.0A, V_{GS}=10V (Note 2,3)	--	16.3	--	nC
Gate-Source Charge	Q_{gs}		--	2.86	--	
Gate-Drain Charge	Q_{gd}		--	8.55	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	7.0	A
Pulsed Source Current	I_{SM}		--	--	25	
Diode Forward Voltage	V_{SD}	I_S=7.0A,V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=7.0A,V_{GS}=0V, dI_F/dt=100A/μs	--	327	--	ns
Reverse Recovery Charge	Q_{rr}		--	2.7	--	μC

Notes:

1. L=30mH, I_{AS}=3.9A, V_{DD}=100V, R_G=25Ω, starting T_J=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

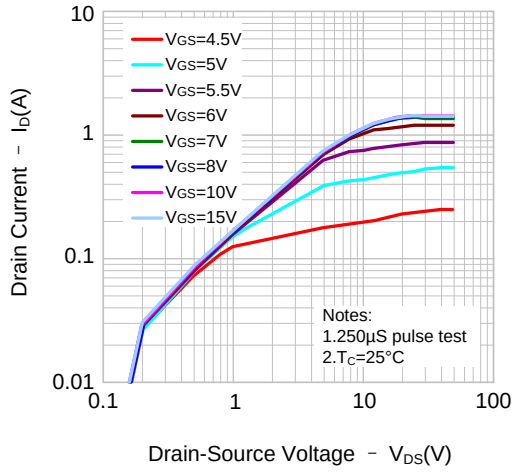


Figure 2. Transfer Characteristics

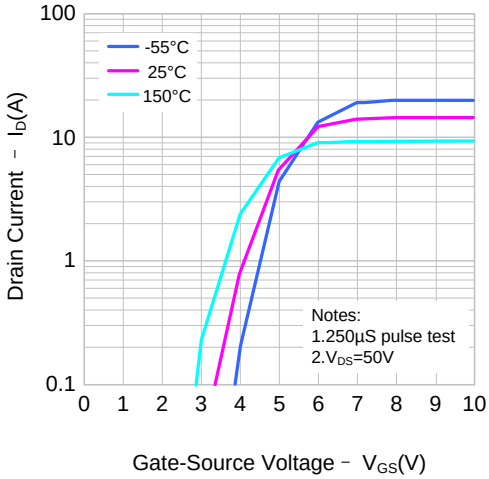


Figure 3. On-Resitance Variation vs. Drain Current and Gate Voltage

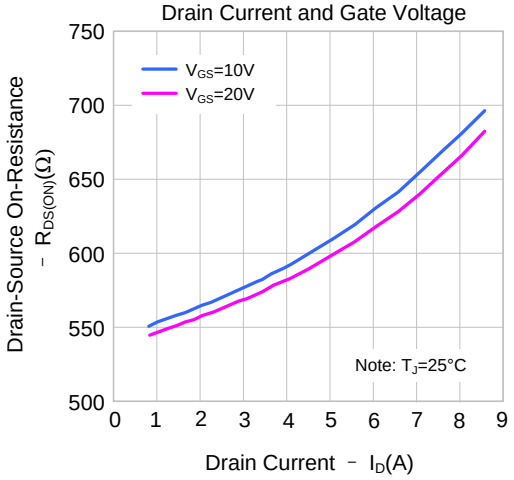


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

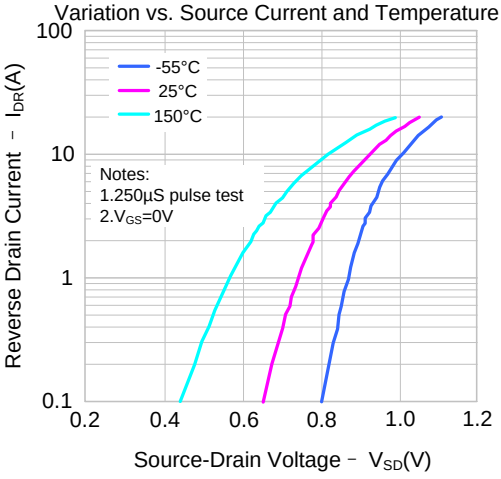


Figure 5. Capacitance Characteristics

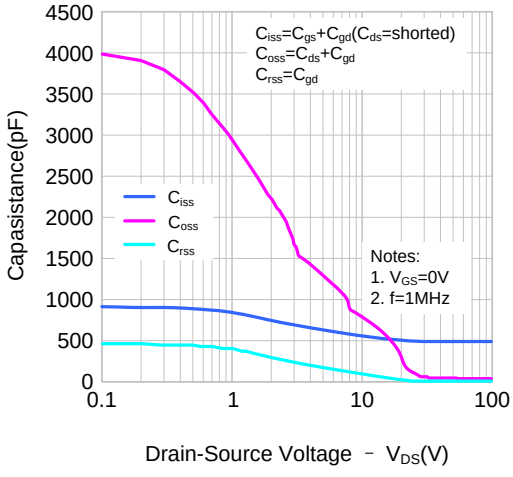
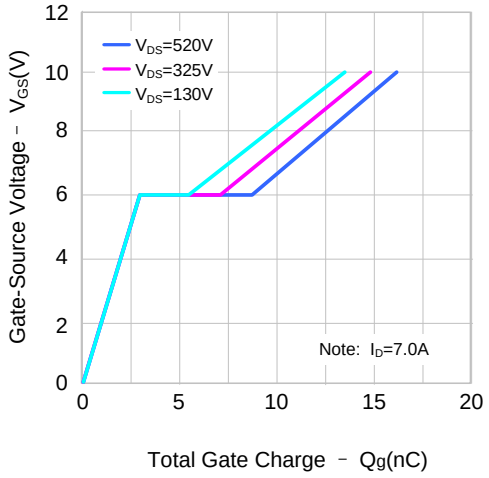


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS(continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

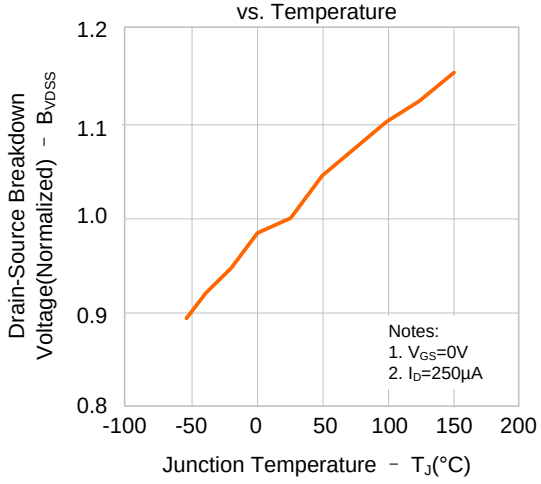


Figure 8. On-resistance Variation vs. Temperature

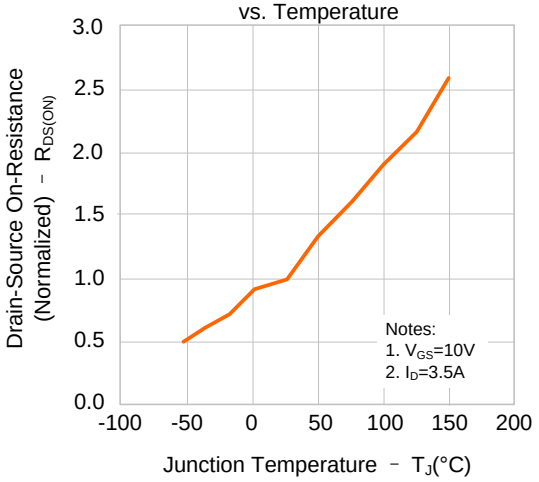


Figure 9-1. Max. Safe Operating Area(SVS7N65F)

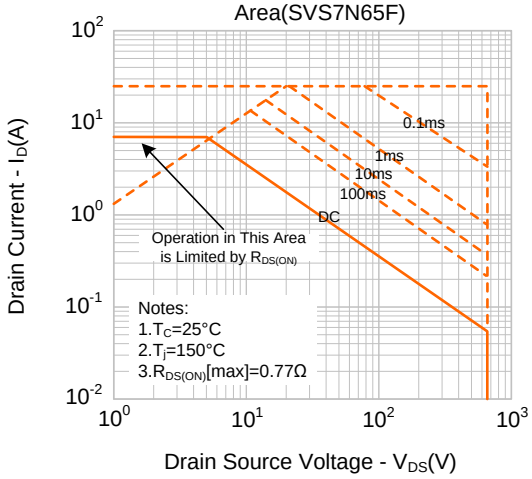


Figure 9-2. Max. Safe Operating Area(SVS7N65D)

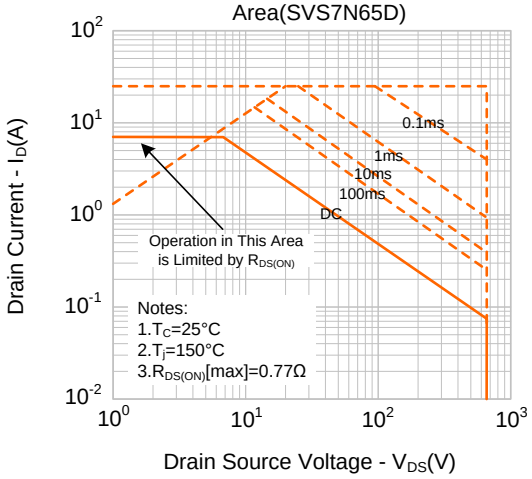
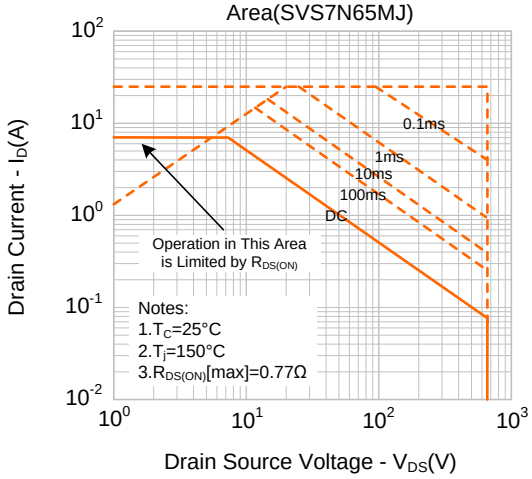
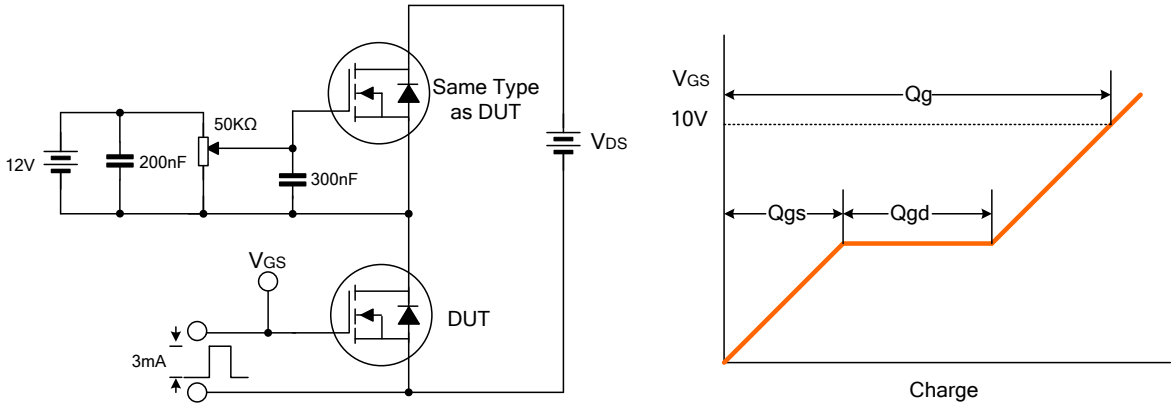


Figure 9-2. Max. Safe Operating Area(SVS7N65MJ)

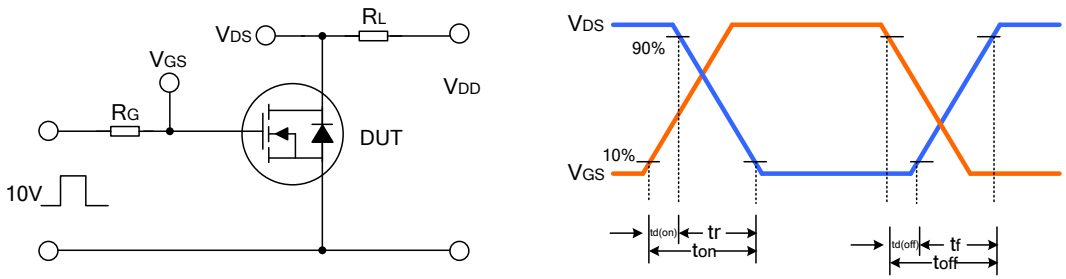


TYPICAL TEST CIRCUIT

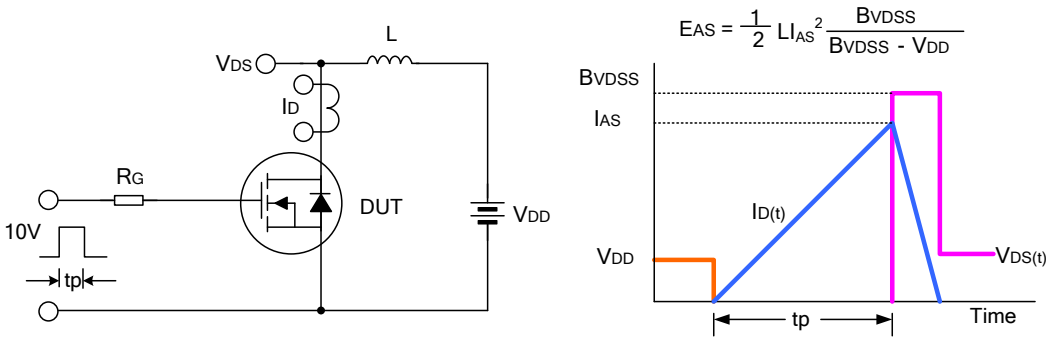
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform

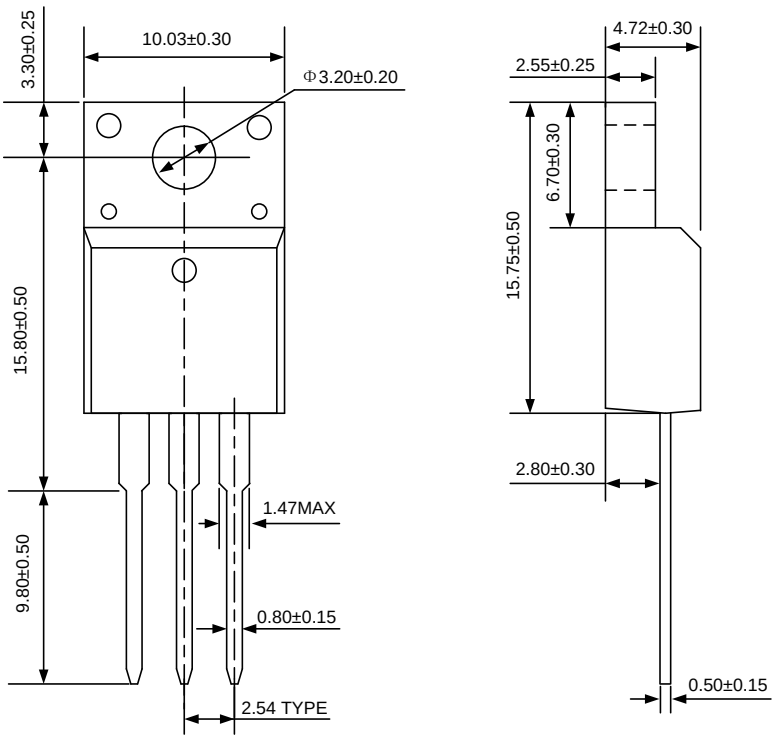


Unclamped Inductive Switching Test Circuit & Waveform

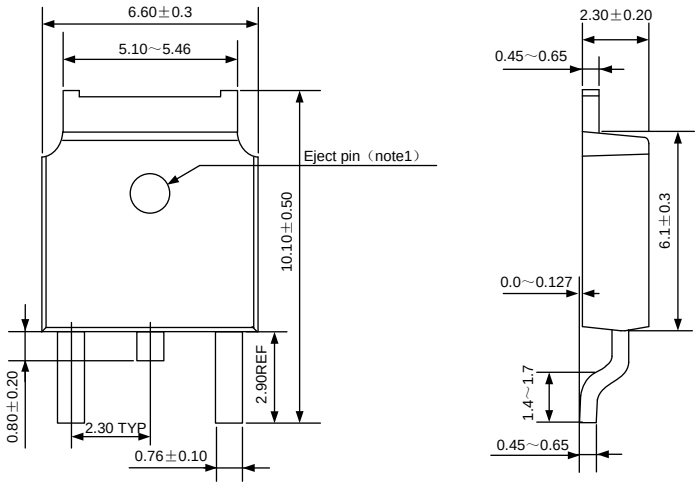


PACKAGE OUTLINE (continued)

TO-220F-3L **UNIT: mm**



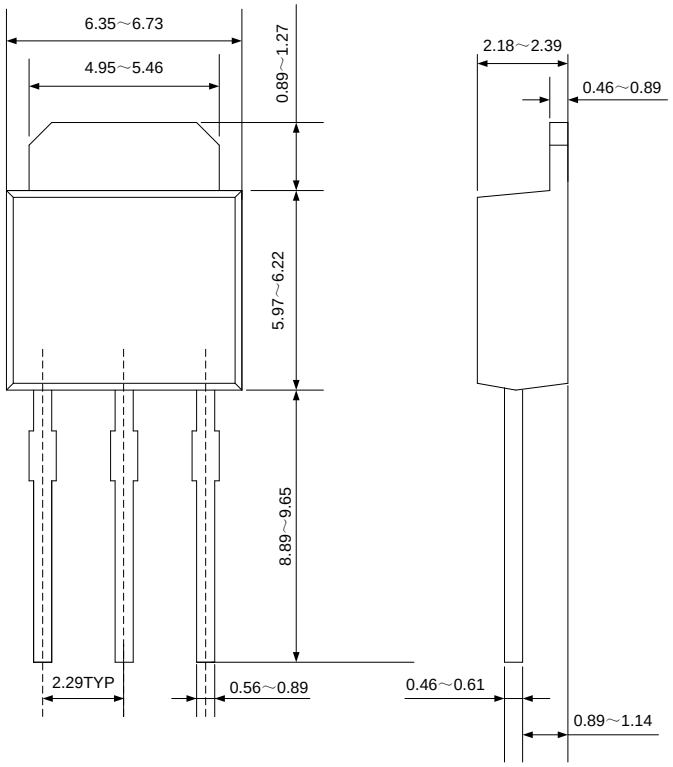
TO-252-2L **UNIT: mm**



NOTE1：There are two conditions for this position:has an eject pin or has no eject pin.

PACKAGE OUTLINE (continued)

TO-251J-3L **UNIT: mm**



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1. First release