ORIENTAL
SEMICONDUCTOR

# GreenMOS™

# Application Note

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# 1. PowerMOSFET and Super-Junction Power MOSFET

Metal-oxide-semiconductor field-effect transistor (MOSFET) is the basic unit in the integrated circuit design, its circuit symbols and device structure shown in Figure 1. A typical n-channel MOS device has four electrodes and connected to a different voltage bias. In general, the source and substrate are connected to low voltage, such as ground. When the device is not working, the device is in the off state, at this time there is no conductive channel between the source and the drain of the device, which is equivalent to the open state of the switch. When the gate is applied with a positive voltage greater than Vgs (th), the p-type substrate surface beneath the gate oxide layer produces an inversion layer, i.e., a via channel. Channel connected to the device source and drain, then nMOS corresponding to the conduction state. The higher the gate voltage, the more conductive the channel becomes.

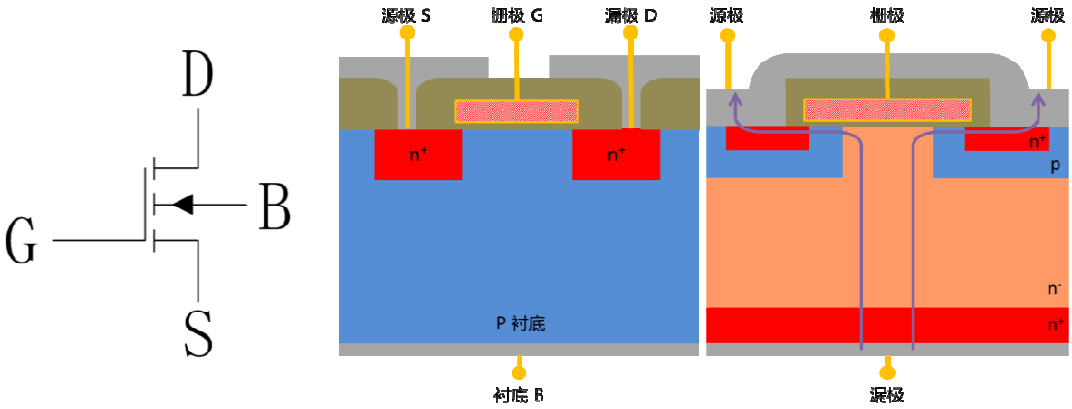



Fig.1 MOSFET Basic StructureFig.2 VDMOS Structure

The high-voltage power MOSFET is usually uses vertical channel structure, as shown in Figure 2, the drain is at the bottom of the chip, the source is at the top of the chip. The device is placed vertically. This structure is called Vertical Double-diffusion MOS (VDMOS). Structurally, the drain of the VDMOS is moved from the original surface to the bottom of the device. The drain current also flows from the

bottom of the device to the surface of the device and becomes a vertical device. The area between the drain current and the channel is the drift region, which is the main part of the voltage used by the high voltage power device. The higher the drift region and the lower the resistivity in the drift region, the higher the voltage it can withstand, and the higher the turn-on resistance of the device. This is because VDMOS Rdson and BVdss is calculated based on Equation 1 : Rdson = a* $BV^{2\sim2.5}$

The use of super-junction MOSFET can break this limit, the basic structure shown in Figure 3. The biggest difference between SJMOS and VDMOS is that the p-pillars are added below the pbody so that alternating pn junctions appear in the drift region. Using the principle of depletion between adjacent pn columns, the concentration of the drift region can be increased, resulting in a decrease in resistivity when the device is turned on. In the off state, the p-pillar and the n-pillar can be depleted from each other, allowing the depletion area to expand as much as possible, maintaining a high withstand voltage, thereby breaking the silicon limit of Equation 1, making the on-resistance and breakdown Voltage to achieve a similar linear relationship, significantly improve the performance of the device.

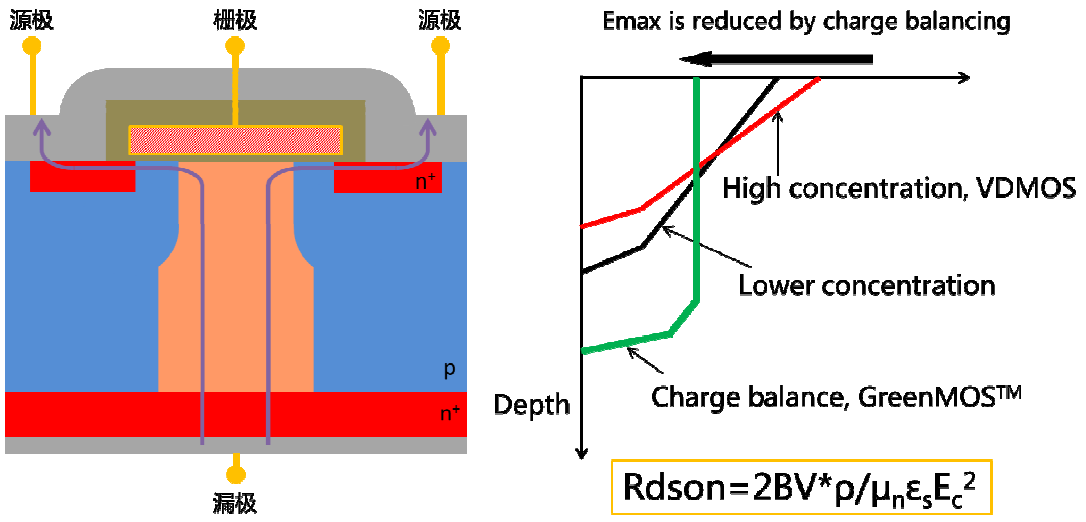



Fig. 3 SJ VDMOS Structure

Compared to ordinary VDMOS devices, the super-junction power device is faster and its FOM is lower. But this also bring some other negative problems, such as high di/dt & dv/dt that can causethe **gate oscillation** and **EMI problems**. Therefore, the super-junctionMOSFET is very particular about the circuit design to avoid it's fast switching that leads to the chip oscillation and results in EMI over spec or even device breakdown.

# 2. GreenMOS™ Technology

The GreenMOS™family of products is a new type of Super-Junction power device from Oriental Semiconductor. The Word of “Green” meaning GreenMOS™itself as a high-quality "green" products, using GreenMOS™can achieve green design and access to green energy products. GreenMOS™series of products covers the Vds voltage range of 500 ~ 900V and Ids range of 1A - 100A with a various types of packagin. As a result of the use of a number of patented technologies, GreenMOS™series of products successfully improves the conventional SJMOS’s EMI issues and the performance reached even better level than the world-class brand, significantly exceeds general power device suppliers. Compared to other companies' super-junction devices, the Oriental Semiconductor’s GreenMOS™has the advantages of "fast switching and less oscillation", its features are as follows:

## 1. Soft Switching

GreenMOS™The manufacturing process of the conventional super-junction power device has been optimized to make the impurity distribution and capacitance inside the device more suitable for the high-speed switching operation of the external circuit, reducing the ripple noise and the voltage spike, and the resulting switch The waveform is more smooth, as shown in Figure 4, the switch during the gate oscillation is lower, is conducive to the improvement of EMI.

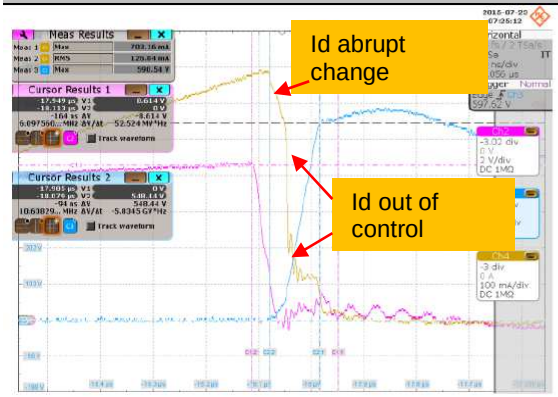
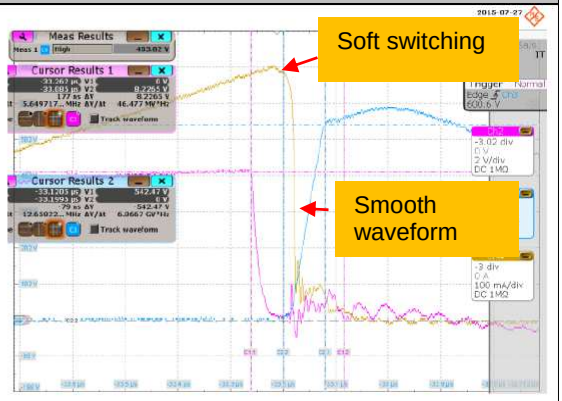
| Conventional super-junction MOSFET | soft-trench SJMOS GreenMOS™ |
|---|---|
| Figure5 : Input Voltage:264Vac&Output:Full Load | Figure6 : Input Voltage:264Vac&Output:Full Load |
|  |  |
| CH2:$V_{GS}$ CH3:$V_{DS}$ CH4:$I_D$<br>GS-$T_{FALL\ TIME}$:164ns DS-$T_{RISE\ TIME}$:94ns | CH2:$V_{GS}$ CH3:$V_{DS}$ CH4:$I_D$<br>GS-$T_{FALL\ TIME}$:177ns DS-$T_{RISE\ TIME}$:79ns |

Fig. 4 Comparison of Switching Oscillation between Conventional SJMOS and GreenMOS™

## 2. Shorter Miller Plateau

Miller Capacitor ( Cgd ) is an important intrinsic parameter that affects the super-junction power device. Many important parameters such as dynamic loss, Qg, tr, tf and so on are related to it. Miller capacitance is reflected in the switching waveform for the performance of the Miller Plateau. As shown in Figure 5a. GreenMOS™series devices use a special design method, the Cgd value per unit area than conventional super-junction power devices reduced by more than 1/3, in order to obtain faster switching time and smaller Qg.

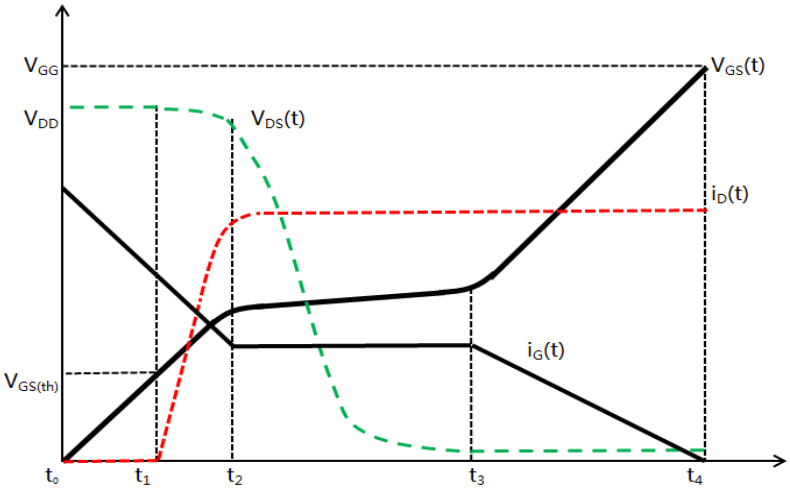



Fig.5aTurn on process andMiller Plateau

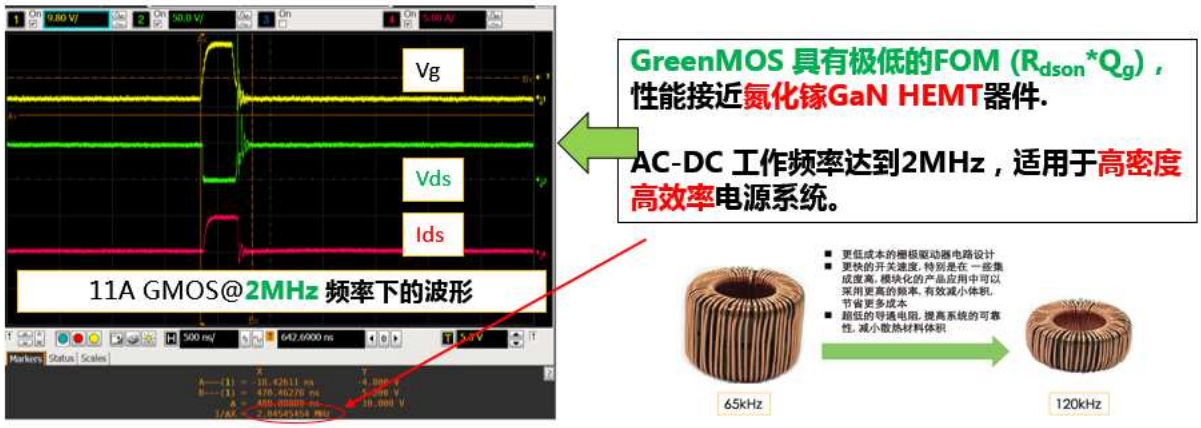



Fig.5bGreenMOS™@ 2MHz Switching

## 3. Low FOM

FOM (Figure of merit) is an important criterion for measuring the merits of power device design. The formula is Rdson * Qg. The smaller the FOM indicates the better switching performance of the device. The GreenMOS™series optimizes the manufacturing process and design of the device. On the one hand, the Qg is reduced by a unique design method. GreenMOS™has the industry-leading FOM value. Due to the excellent FOM characteristics of GreenMOS™,itsdynamic losses can be reduced to 2/3 of the conventional super-junction devices.It can be operated at more than 2MHz switching frequency. The switching speed is close to the high-end third-generation semiconductor devices - high-voltage GaN power devices (see Figure 5b).

# 3. GreenMOS™Driver Circuit Optimization

## 1. EMI improvement when replacing Planar MOSFETs

The GreenMOS™has extremely low FOM (Qg * Rdson) and gate capacitance to reduce switching losses. When replacing traditional VDMOS withGreenMOS™on some systems, below key items need to be noted:

1) Oriental Semiconductor uses its unique patented technology, greatly reducing the GreenMOS™gate charge (Qg), improve the switching efficiency. Since the switching speed of the GreenMOS™is far greater than that of the conventional VDMOS, the value of the gate drive resistorshould be increased when replacing the VDMOS to reduce the switching speed, thereby reducing the gate oscillation, the voltage pulse spike and oscillation.

2) Since GreenMOS™is specially optimized at the device level, its EMI margin is better than the conventional super-junction MOSFET. Due to its extremely low switching losses, the system can maintain a higher efficiency, lower temperature rise than VDMOS even after increasing the gate resistance.

3) In the practical application of GreenMOS™, the drive parameters in accordance with the “slow turn-on, fast close” principle, to enhance the system performance and reliability.

## EMIDebug Guide

1) When replacing ordinary VDMOS, if you are using a single gate resistor to drive the MOSFET, you can increase the drive resistance, and the need to balance the efficiency, as shown in Figure 6.

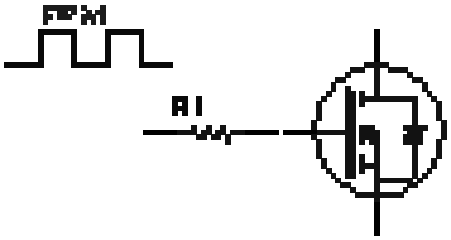



Fig. 6

a, GreenMOS™ current between 2A ~ 4A, the drive resistance increases the approximate range of 100Ω ~ 200Ω

b, GreenMOS™ current between 5A ~ 20A, the drive resistance increases in the approximate range of 75Ω ~ 150Ω

c, GreenMOS™ current between 23A ~ 78A, the drive resistance increases in the approximate range of 15Ω ~ 51Ω

2) When replacing of ordinary VDMOS, if the gate driver is configured as below, you can increase both theturn-on resistance turn-off resistance.

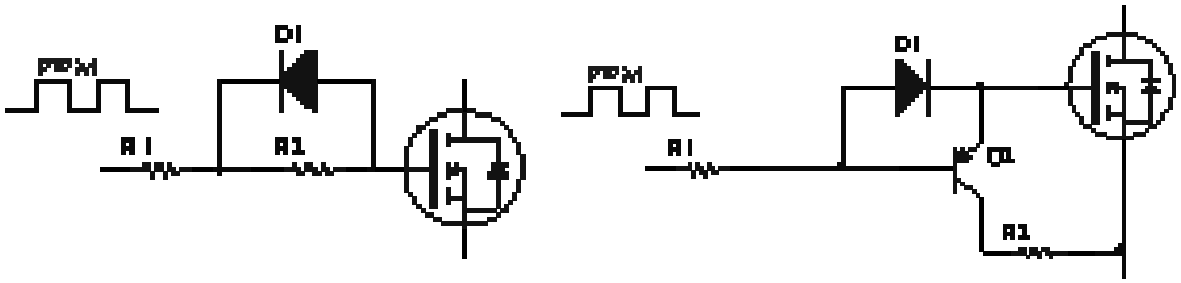



Fig.7Fig.8

a, Figure 7 drive mode, GreenMOS™ current between 2A ~ 4A, the resistance R1 + R2 increases the approximate range of 200Ω ~ 400Ω, the resistance R1 increases the approximate range of 100Ω ~ 200Ω

b, Figure 7 drive mode, GreenMOS™ current between 5A ~ 8A, the resistance R1 + R2 increases the approximate range of 150Ω ~ 450Ω, the resistance R1 increases the approximate range of 75Ω ~ 150Ω

c, Figure 7 drive mode, GreenMOS™ current between 11A ~ 20A, the resistance R1 + R2 increases the approximate range of 100Ω ~ 200Ω, the resistance R1 increases the range of 51Ω ~ 150Ω

d, Figure 7 drive mode, GreenMOS™ current between 23A ~ 78A, the resistance R1 + R2 increases the range of 51Ω ~ 100Ω, the resistance R1 increases the approximate range of 10Ω ~ 51Ω

e, Figure 8 drive mode, GreenMOS™ current between 2A ~ 4A, the resistance R1 increases the approximate range of 200Ω ~ 400Ω, resistance R2 debugging the general range of 100Ω ~ 200Ω

f, Figure 8 drive mode, GreenMOS™ current between 5A ~ 8A, the resistance R1 increases the range of 150Ω ~ 450Ω, the resistance R2 increases the approximate range of 75Ω ~ 150Ω

g, Figure 8 drive mode, GreenMOS™ current between 11A ~ 20A, the resistance R1 increases in the approximate range of 100Ω ~ 200Ω, the resistance R2 increases the approximate range of 51Ω ~ 150Ω

h, Figure 8 drive mode, GreenMOS™ current between 23A ~ 78A, the resistance R1 increases the range of 51Ω ~ 100Ω, the resistance R2 increases the approximate range of 10Ω ~ 51Ω

### 3) EMI Further Debug

a, If the EMI margins are still insufficient after increasing the drive resistance, we can add magnetic beadsto GreenMOS™'s source pin, adjust the RCD absorption circuit parameters and add magnetic beads to the absorption circuit of the diode pins or add high-V capacitors (51pF / 1000V or 100pF / 1000V) between the D/S pins.

b, adjust the input and output of the common mode inductance, inhibit the corresponding frequency segment of the common mode interference.

c, adjust the Y parameters and the connection points.

d, if necessary, adjust the secondary Schottky RC absorption circuit parameters or increase the magnetic beads to suppress the corresponding frequency segment.

e, adjust the winding order of the transformer, such as the moving point as a winding point around the system.

f, When replacing ordinary VDMOS, if the original driving scheme is totempole. We can get rid of the totem pole and using single resistor for the gate driver.

Note: The range of drive resistance parameters if for reference only. In the actual applications, it should be tested to according to the application topology, PWM chip drive capability, efficiency, temperature, EMI, PCB Layout and other factors. Do the appropriate debugging, even with the same parameters of the GreenMOS™, in different applications, the drive resistance may also be different.

## 2. Electrostatic Protection

Strengthen the electrostatic protection measures to prevent the device failure due to the ESD, SJMOS may be sensitive to ESD compared to VDMOS due to smaller Cgd/Cds.

## 3. Gate Oscillation

In the actual operation, GreenMOS™is in a high-speed opening and closing working state. In this high-frequency switching process it will likely cause gate oscillation.

**a, select the appropriate gate drive resistor**

The small gate resistance causes the GreenMOS™to turn off quickly, and the energy stored in the gate and gate inductors cannot be drained immediately, causing GreenMOS™ fail to operate normally, resulting in a oscillation. Causing the GreenMOS™gate oxide layer to be damaged.We can use the oscilloscope to observe the switching waveform and appropriately increase the gate drive resistance.

**b, the use of magnetic beads to suppress the gate oscillation**

At higher frequencies, adding the magnetic beads can suppress spikes in the absorption circuit. For SMT type of devices (TO252/TO263), we can add the beads between the gate resistor and the gate. For the DIP type devices, we can add the bead to the gate pin to effectively prevent the parallel run crosstalk problem.

**c, optimize the PCB wiring**

Make the gate wiring as short as possible, and place the gate drive resistor close to the gate of the GreenMOS™. It reduces parasitic inductance and eliminates interference. But also need to pay attention to avoid the gate-drain and the gate-high voltage wires are too close that may cause short circuit. And to ensure that the gate / drain does not appear parallel to the line. If the circuit layout is special, consider the use of ground wire gate shielding isolation.

## 4. Draining Resistor

In practical applications, we can add draining resistor between the gate and source of the GreenMOS™. The general resistance value is about 10kohm, shown in Figure 9, resistance R2.

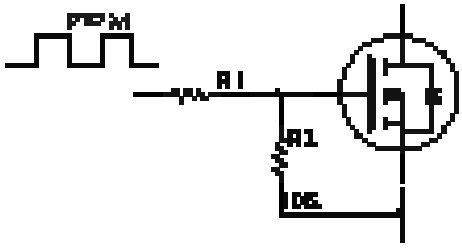


Fig. 9

## 5. Avalanche Breakdown

If the drain and the source of GreenMOS™undertakes surge voltage exceeds the breakdown voltage of BVdss, GreenMOS™can withstand a certain amount of impact.The impact energy can be referenced to the EAS value and EAR value in the datasheet. Excessive impact energy will cause GreenMOS™to fail. In the case of power-on/off, hot swapping, short circuit, the impact voltage should not exceed the minimum value of the GreenMOS™rated parameter BVdss. In the case of thederating, the maximum voltage after the steady state cannot exceed 80% of the rated voltage.

**Precautions to reduce the impulse voltage:**

a, Using large and short wiring for the high current path. Reduce the loop area, and reduce the parasitic inductance

b, Increasing the gate driver resistance and add high-V capacitor between the gate and drain of the GreenMOS™ to reduce dv/dt

c, Using appropriate transformer winding mode and the transformer reflection voltage design

As shown in Figure 10, for a smaller gate drive resistor, the Vds maximum voltage exceeds the rated breakdown voltage of BVdss=650V, leads to potential risk of failure. After increasing the gate resistance, the problem is solved.

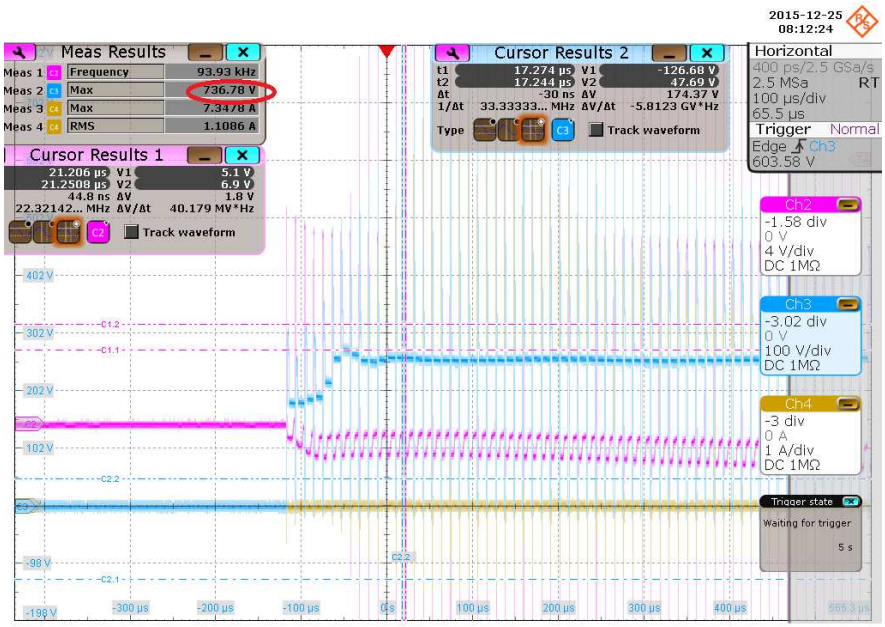



Fig. 10

d, adjusting the RC absorption circuit, and in the wiring, try to reduce the loop area and make it close to the drain and source of the GreenMOS™as shown in Figure 11

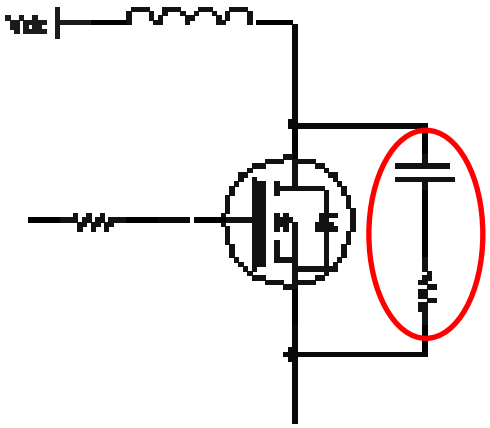


Fig. 11

e, adjust the RCD absorption circuit, and in the wiring, try to reduce the loop area and to make it close to the GreenMOS™drain and the transformer, as shown in Figure 12.

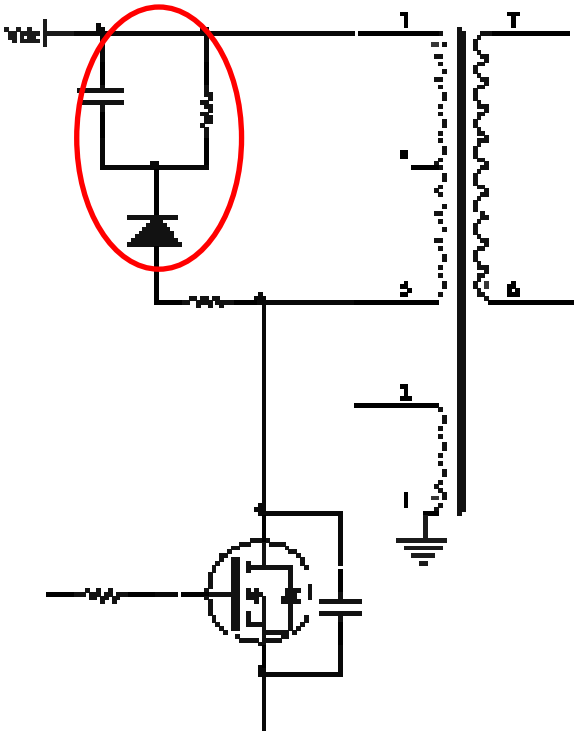


Fig. 12

## 6. Safe Operation Area ( SOA )

If the drain current Id, the drain and source voltage Vdss andthe power Pw exceed the maximum rating of the device, the device may be failure caused by heat generation beyond the safe working area. The causes of failure are due to:

a, Overheat Continuity: Excessive DC power caused by conduction loss induced by on-state resistance Rds (on) and leakage current.

b, Excessive Reason: pulse current beyond the safe working area, the load short circuit beyond the safe working area, switching losses, body diode Trr loss, all related to the overheat of the device.

Parasitic inductance and parasitic capacitance to produce large L * dI / dt and C * dV / dt, will also seriously affect the safety of GreenMOS™. Therefore, the parasitic parameters of the gate drive circuit, the parasitic parameters of the drain circuit, the parasitic parameters between the drain and the gate should be strictly controlled to ensure that GreenMOS™works in the safe working area.

## 7. GreenMOS™in Parallel Use

When using high-speed GreenMOS™ in parallel applications, we should pay attention to dynamic current balancing and gate synchronization/oscillation.

Note:

a, In PCB wiring, it requires a lower parasitic inductance and parasitic capacitance

b, each GreenMOS™gate wiring should have the same length and width, and each GreenMOS™has a separate drive resistor, as shown in Figure 13

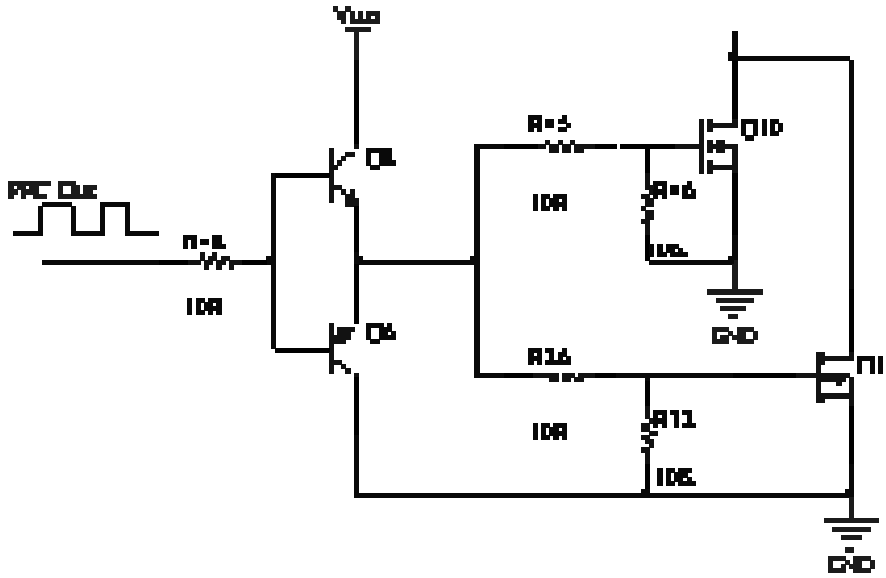


Fig. 13

c, choose GreenMOS™with higherVth in order to avoid oscillation caused by early turn-on by single device.

d, if there is obvious oscillation of the gatescaused by parasitic inductance and parasitic capacitance, it is recommended to add ferrite beads to the gate pins to suppress the oscillations.

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