N-Channel Enhancement Mode Power MOSFET

Description

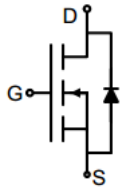
The GT095N10K uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

General Features

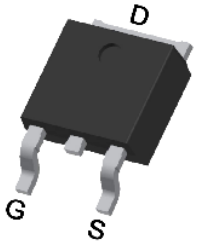
- V_{DS} 100V
- I_D (at V_{GS} = 10V) 73A
- $R_{DS(ON)}$ (at V_{GS} = 10V) < 9.5mΩ
- $R_{DS(ON)}$ (at V_{GS} = 4.5V) < 15mΩ
- 100% Avalanche Tested
- RoHS Compliant

Application

- Synchronous Rectification in SMPS or LED Driver
- UPS
- Motor Control
- BMS
- High Frequency Circuit



Schematic Diagram



TO-252

Device	Package	Marking	Packaging
GT095N10K	TO-252	GT095N10	2500pcs/Reel

Absolute Maximum Ratings T_C = 25ºC, unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	100	V
Continuous Drain Current	I_D	73	A
Pulsed Drain Current (note1)	I_{DM}	290	A
Gate-Source Voltage	V_{GS}	±20	V
Power Dissipation	P_D	104	W
Single pulse avalanche energy （note3）	E_{AS}	7.5	mJ
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	ºC

Thermal Resistance

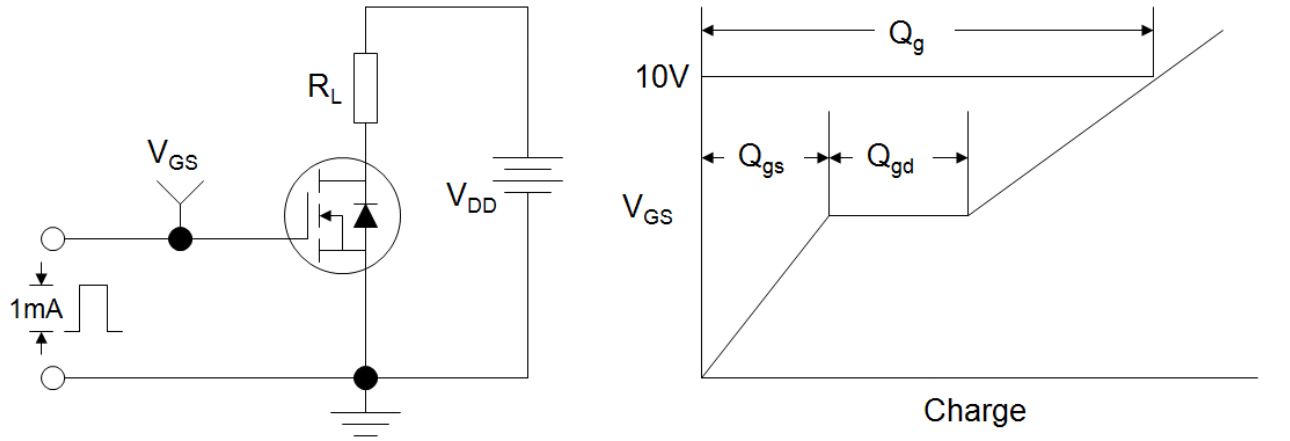
Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	R_{thJC}	1.2	ºC/W
Thermal Resistance, Junction-to-Ambient	R_{thJA}	50	ºC/W

Specifications T_J = 25ºC, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Value**			**Unit**
			Min.	**Typ.**	**Max.**	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	100	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100V, V_{GS} = 0V	--	--	1	μA
Gate-Source Leakage	I_{GSS}	V_{GS} = ±20V	--	--	±100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.5	2.1	2.5	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 35A	--	8.6	9.5	mΩ
		V_{GS} = 4.5V, I_D = 35A	--	13	15	
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=20A	--	60	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 50V, f = 1.0MHz	--	2275	--	pF
Output Capacitance	C_{oss}		--	162	--	
Reverse Transfer Capacitance	C_{rss}		--	7.9	--	
Total Gate Charge	Q_g	V_{DS} = 50V, I_D = 14A, V_{GS} = 10V	--	29	--	nC
Gate-Source Charge	Q_{gs}		--	5	--	
Gate-Drain Charge	Q_{gd}		--	5	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 50V, I_D = 14A, R_G = 10Ω	--	8	--	ns
Turn-on Rise Time	t_r		--	3	--	
Turn-off Delay Time	$t_{d(off)}$		--	26	--	
Turn-off Fall Time	t_f		--	4	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	T_C = 25ºC	--	--	73	A
Body Diode Voltage	V_{SD}	T_J = 25ºC, I_{SD} = 35A, V_{GS} = 0V	--	--	1.2	V

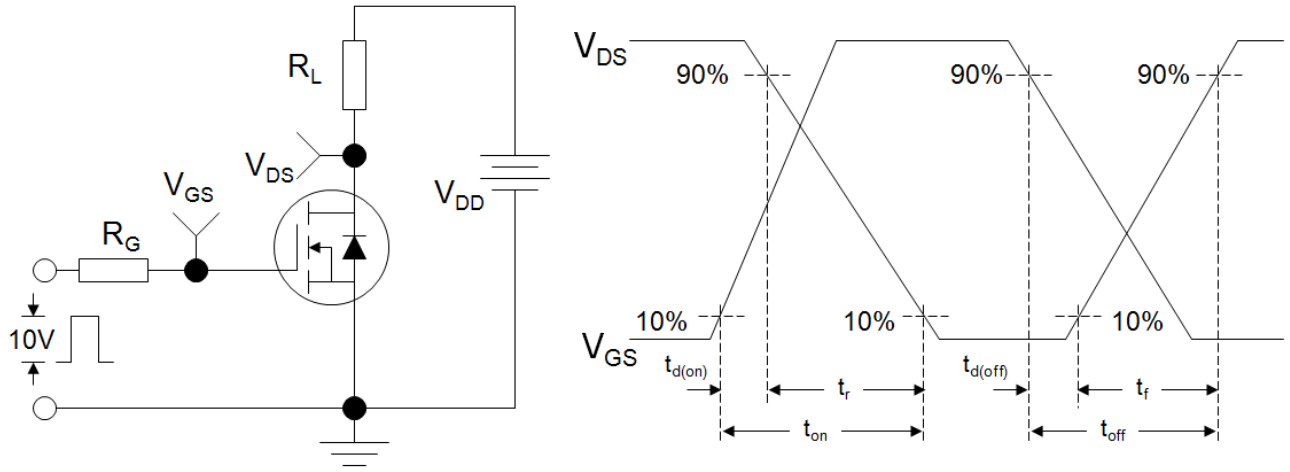
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. Identical low side and high side switch with identical R_G
3. EAS condition : Tj=25℃ ,VDD=50V,VGS=10V,L=0.5mH,Rg=25Ω

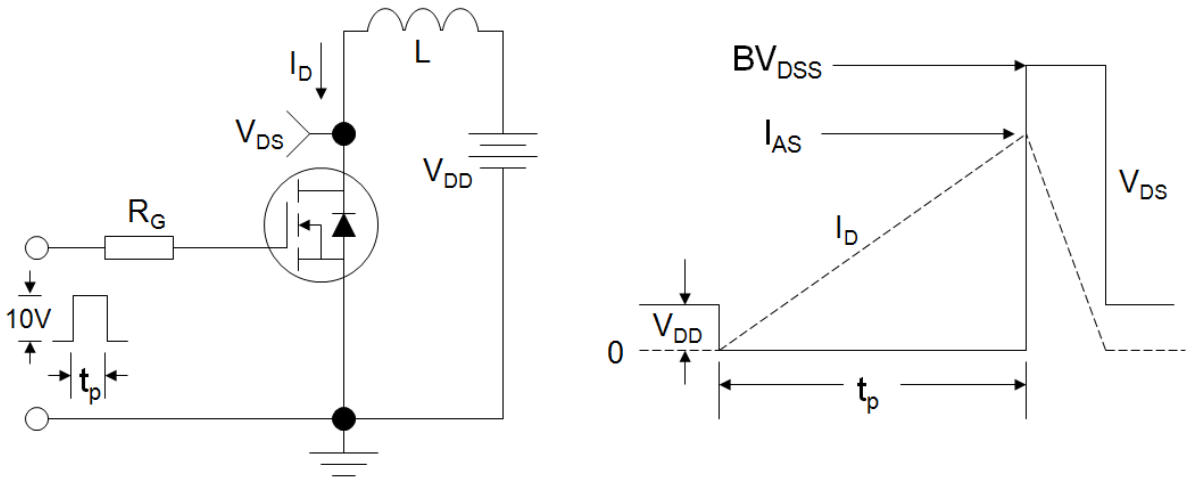
Gate Charge Test Circuit



EAS Test Circuit



Switch Time Test Circuit



Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 1. Output Characteristics

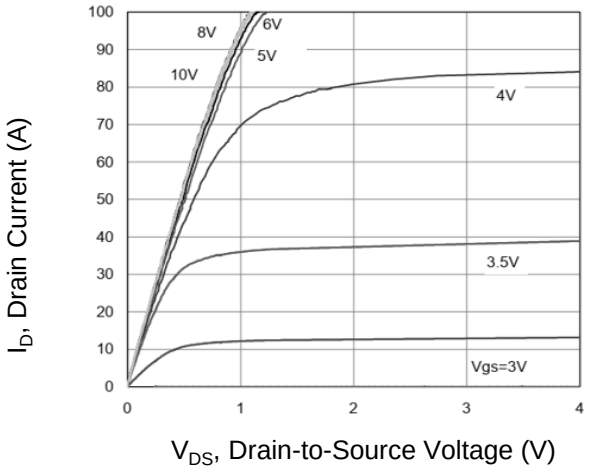


Figure 2. Transfer Characteristics

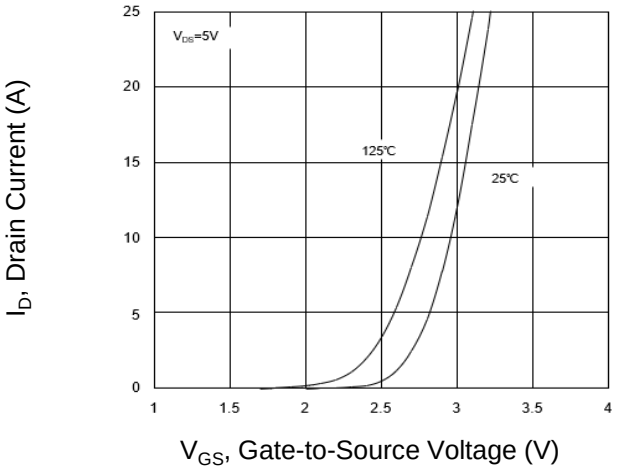


Figure 3. Gate Charge

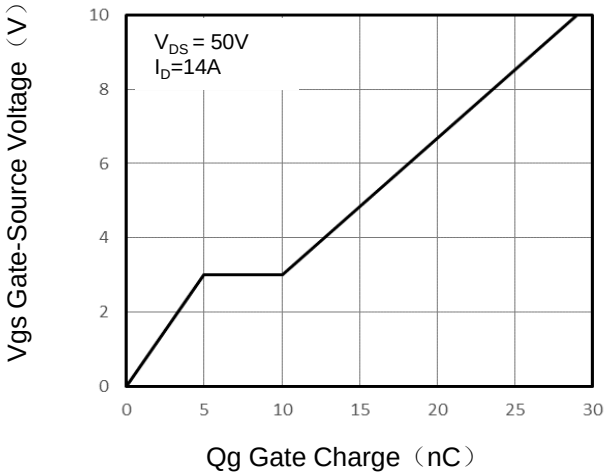


Figure 4. Drain Source On Resistance

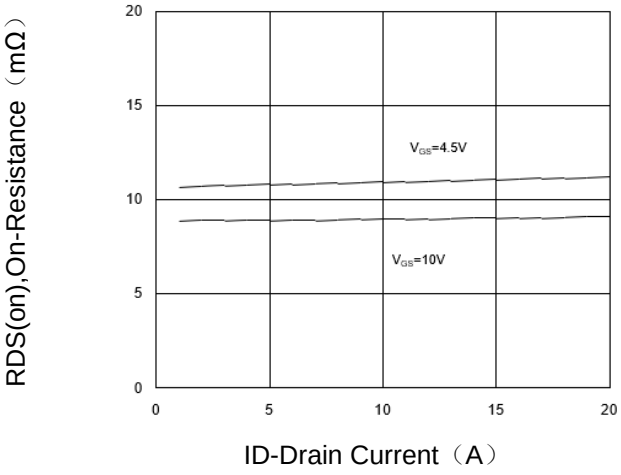


Figure 5. Capacitance vs Vds

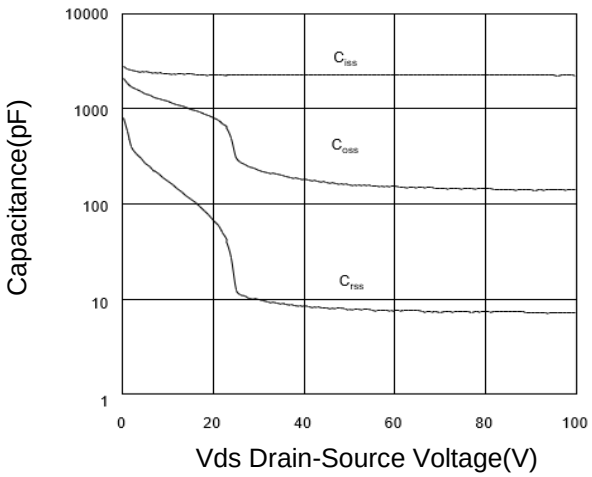
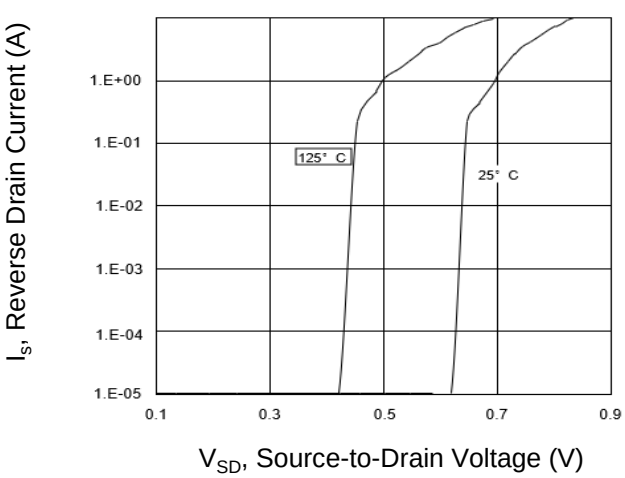
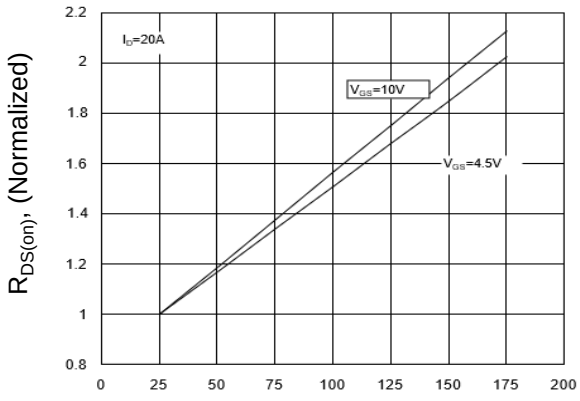


Figure 6. Source-Drain Diode Forward



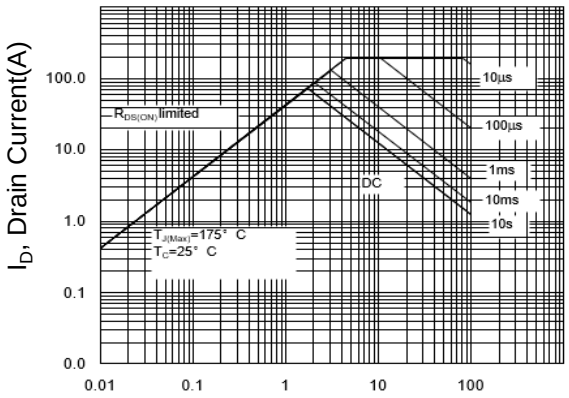
Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 7. Drain-Source On-Resistance



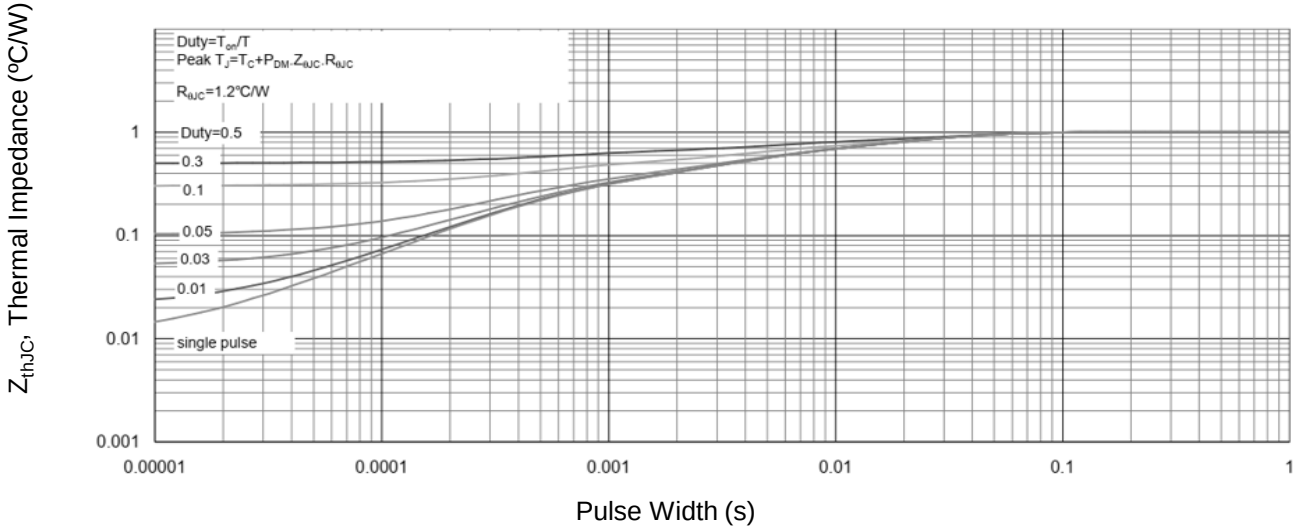
T_J, Junction Temperature (ºC)

Figure 8. Safe Operation Area



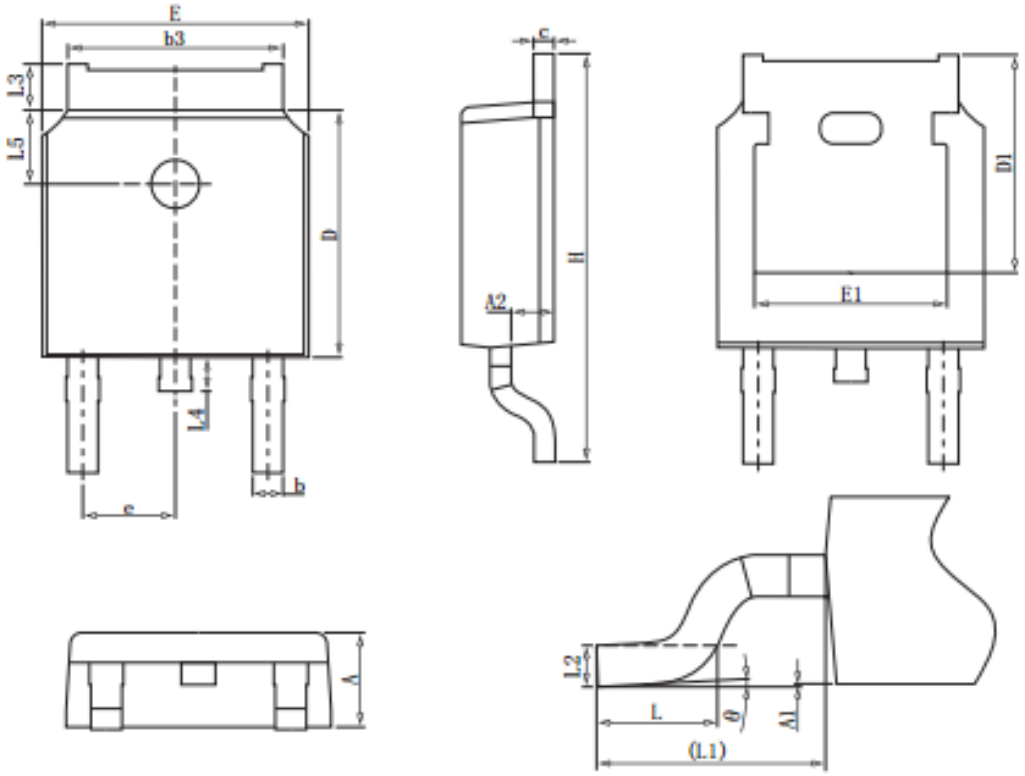
V_{DS}, Drain-Source Voltage(V)

Figure 9. Normalized Maximum Transient Thermal Impedance



Pulse Width (s)

TO-252 Package Information



Symbol	Dimensions in Millimeters		
	MIN.	NOM.	MAX.
A	2.2	2.3	2.4
A1	0		0.2
A2	0.97	1.07	1.17
b	0.68	0.78	0.9
b3	5.2	5.33	5.5
c	0.43	0.53	0.63
D	5.98	6.1	6.22
D1	5.30REF		
E	6.4	6.6	6.8
E1	4.63		
e	2.286BSC		
H	9.4	10.1	10.5
L	1.38	1.5	1.75
L1	2.90REF		
L2	0.51BSC		
L3	0.88		1.28
L4	0.5		1
L5	1.65	1.8	1.95
θ	0°		8°