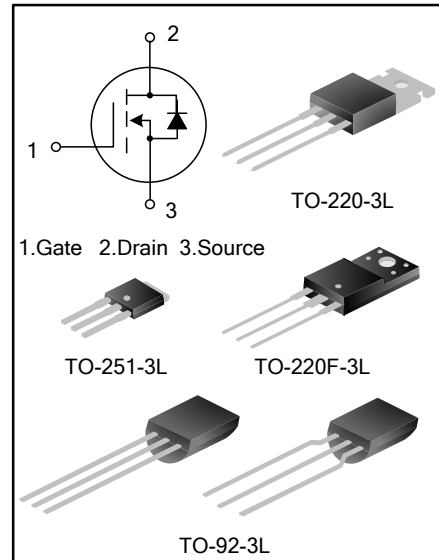


1A, 800V N-CHANNEL MOSFET

GENERAL DESCRIPTION

SVD1N80B/F/M/T is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary S-Rin™ structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

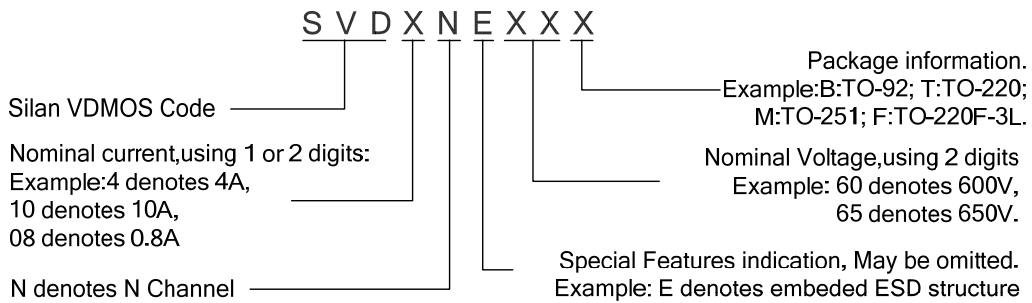
These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.



FEATURES

- * 1A,800V, $R_{DS(on)(typ)}=13.5\Omega@V_{GS}=10V$
- * Low gate charge
- * Low Crss
- * Fast switching
- * Improved dv/dt capability

NOMENCLATURE



ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SVD1N80M	TO-251-3L	SVD1N80M	Pb free	Tube
SVD1N80T	TO-220-3L	SVD1N80T	Pb free	Tube
SVD1N80B	TO-92-3L	1N80B	Pb free	Bulk
SVD1N80BTR	TO-92-3L	1N80B	Pb free	AMMO
SVD1N80F	TO-220F-3L	SVD1N80F	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Characteristics	Symbol	Rating				Unit
		SVD1N80B	SVD1N80F	SVD1N80M	SVD1N80T	
Drain-Source Voltage	V _{DS}	800				V
Gate-Source Voltage	V _{GS}	±30				V
Drain Current	I _D	1.0				A
Drain Current Pulsed	I _{DM}	4.0				A
Power Dissipation(T _C =25°C) -Derate above 25°C	P _D	9	23	33	45	W
		0.07	0.18	0.26	0.36	W/°C
Single Pulsed Avalanche Energy (Note 1)	E _{AS}	23				mJ
Operation Junction Temperature Range	T _J	-55~+150				°C
Storage Temperature Range	T _{stg}	-55~+150				°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Rating				Unit
		SVD1N80B	SVD1N80F	SVD1N80M	SVD1N80T	
Thermal Resistance, Junction-to-Case	R _{θJC}	13.89	4.43	3.79	2.78	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	120	120	110	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B _{VDS}	V _{GS} =0V, I _D =250μA	800	--	--	V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =800V, V _{GS} =0V	--	--	10	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V	--	--	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D =250μA	3.1	--	4.4	V
Static Drain- Source On State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =0.5A	--	13.5	16	Ω
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1.0MHZ	--	160.9	-	pF
Output Capacitance	C _{oss}		--	15.5	-	
Reverse Transfer Capacitance	C _{rss}		--	1.35	-	
Turn-on Delay Time	t _{d(on)}	V _{DD} =400V, I _D =1.0A, R _G =25Ω (Note 2,3)	--	8.13	-	ns
Turn-on Rise Time	t _r		--	15.13	-	
Turn-off Delay Time	t _{d(off)}		--	12.80	-	
Turn-off Fall Time	t _f		--	20.93	-	
Total Gate Charge	Q _g	V _{DS} =640V, I _D =1.0A, V _{GS} =10V (Note 2,3)	--	5.35	-	nC
Gate-Source Charge	Q _{gs}		--	1.28	-	
Gate-Drain Charge	Q _{gd}		--	2.59	-	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	1.0	A
Pulsed Source Current	I_{SM}		--	--	4.0	
Diode Forward Voltage	V_{SD}	$I_S=1.0A, V_{GS}=0V$	--	--	1.5	V
Reverse Recovery Time	T_{rr}	$I_S=1.0A, V_{GS}=0V$, $dI_F/dt=100A/\mu S$ (Note 2)	--	160	--	ns
Reverse Recovery Charge	Q_{rr}		--	0.3	--	μC

Notes:

1. $L=30mH, I_{AS}=1.17A, V_{DD}=110V, R_G=25\Omega$, starting $T_J=25^\circ C$;
2. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycles $\leq 2\%$;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

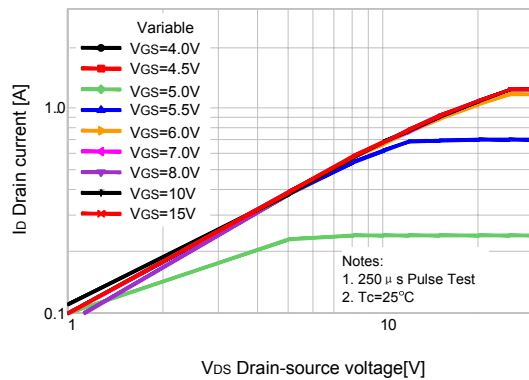


Figure 2. Transfer Characteristics

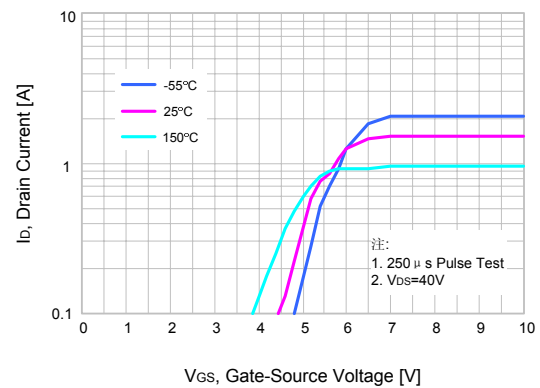


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

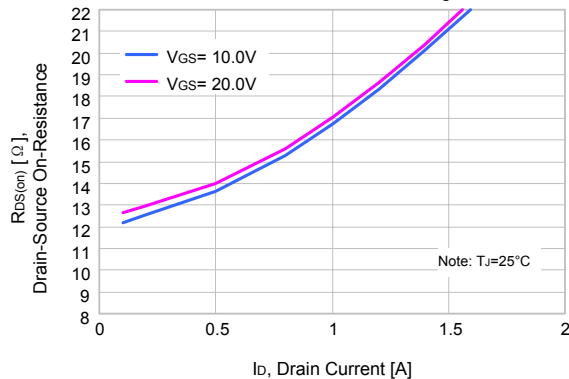
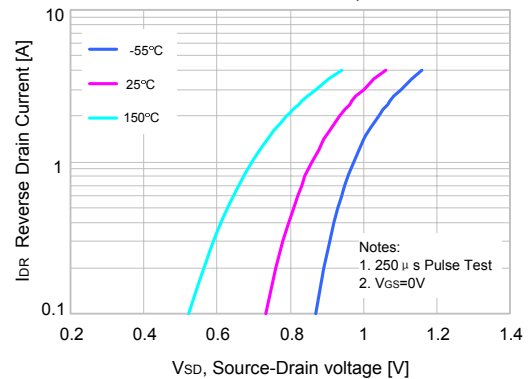


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature



TYPICAL CHARACTERISTICS (continued)

Figure 5. Capacitance Characteristics

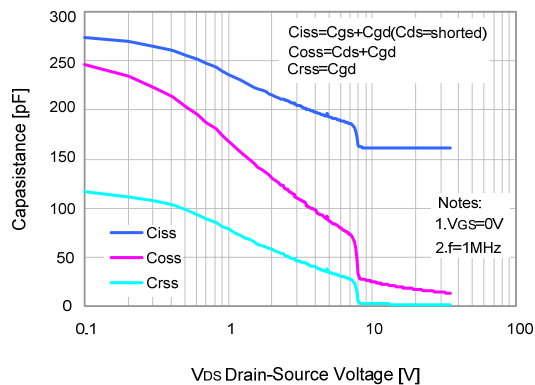


Figure 6. Gate Charge Characteristics

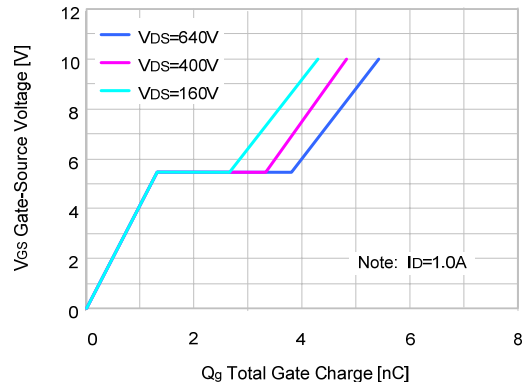


Figure 7. Breakdown Voltage Variation vs. Temperature

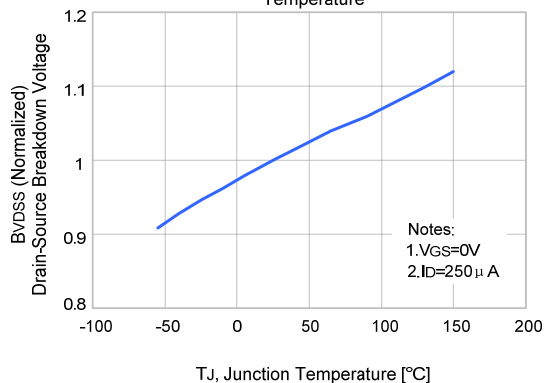


Figure 8. On-resistance Variation vs Temperature

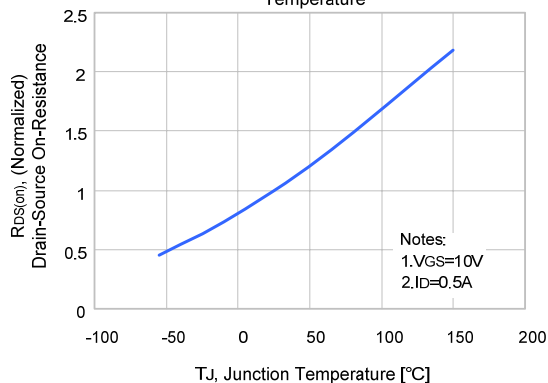


Figure 9-1. Max. Safe Operating Area(SVD1N80B)

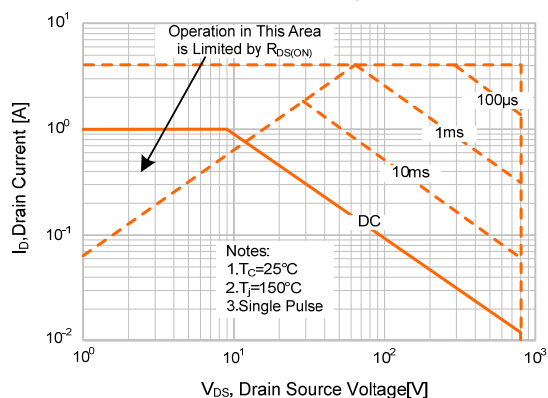
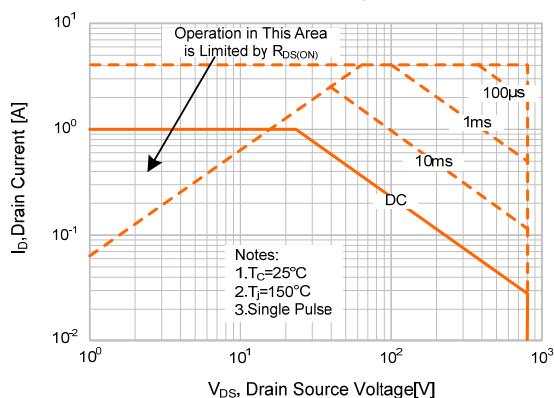
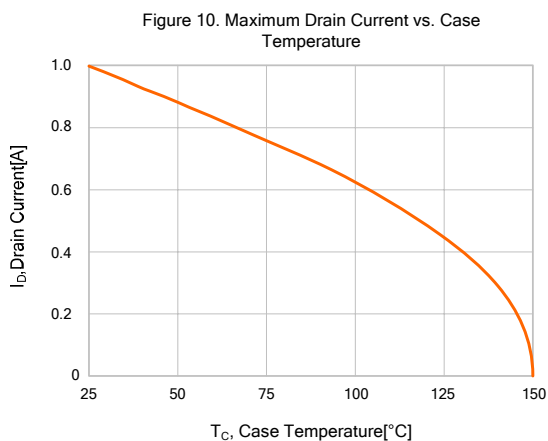
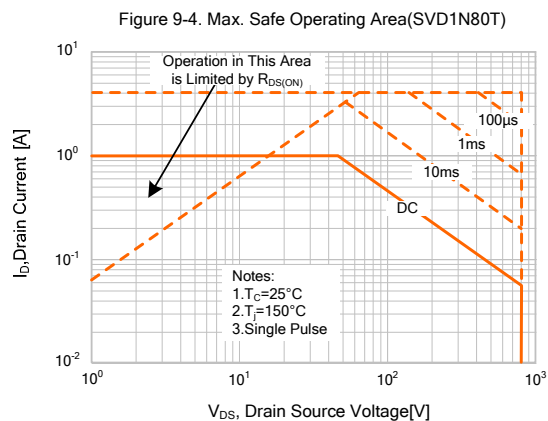
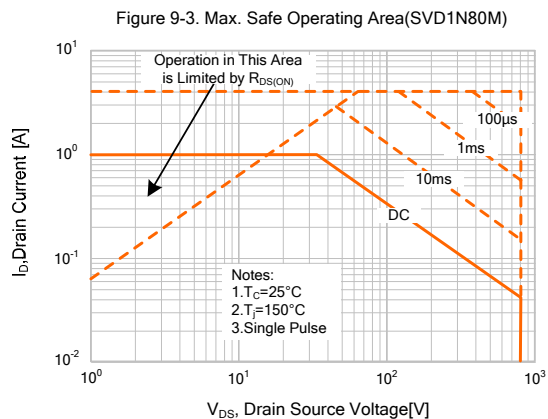


Figure 9-2. Max. Safe Operating Area(SVD1N80F)

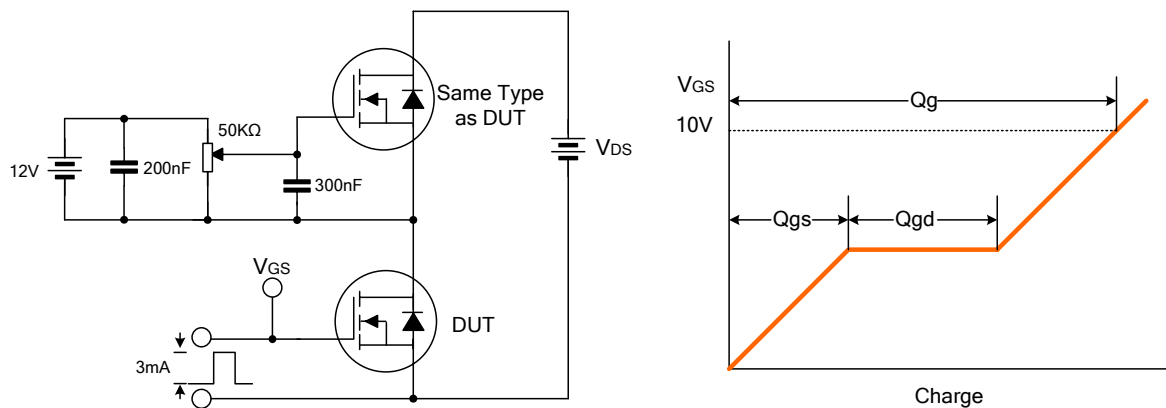


TYPICAL CHARACTERISTICS (continued)

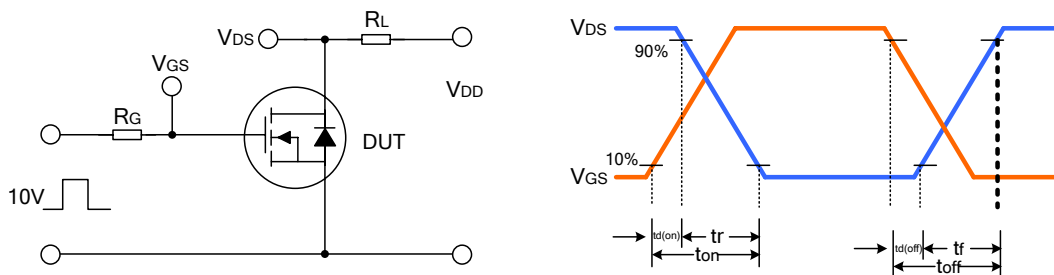


TYPICAL TEST CIRCUIT

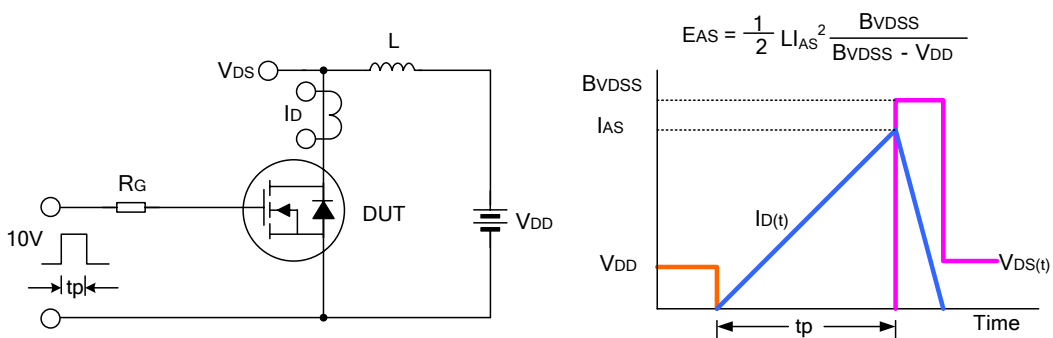
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



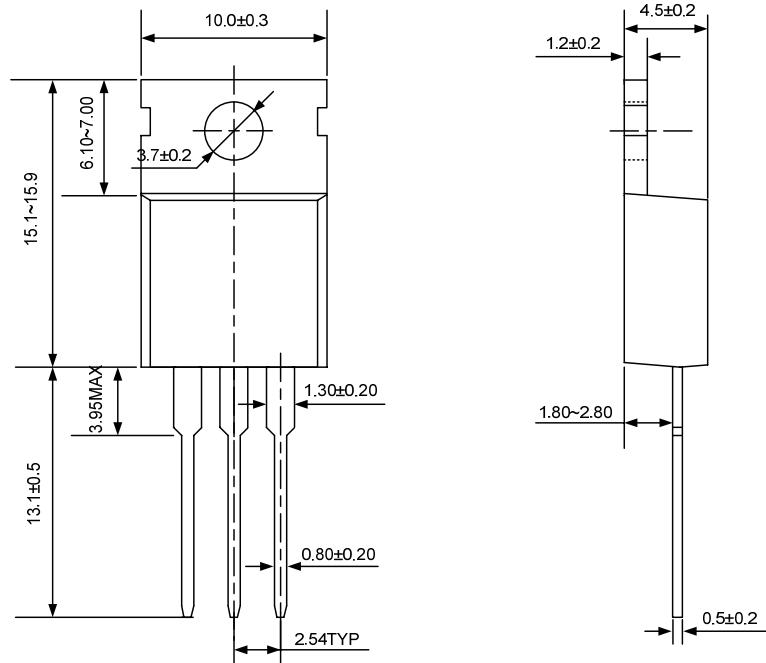
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

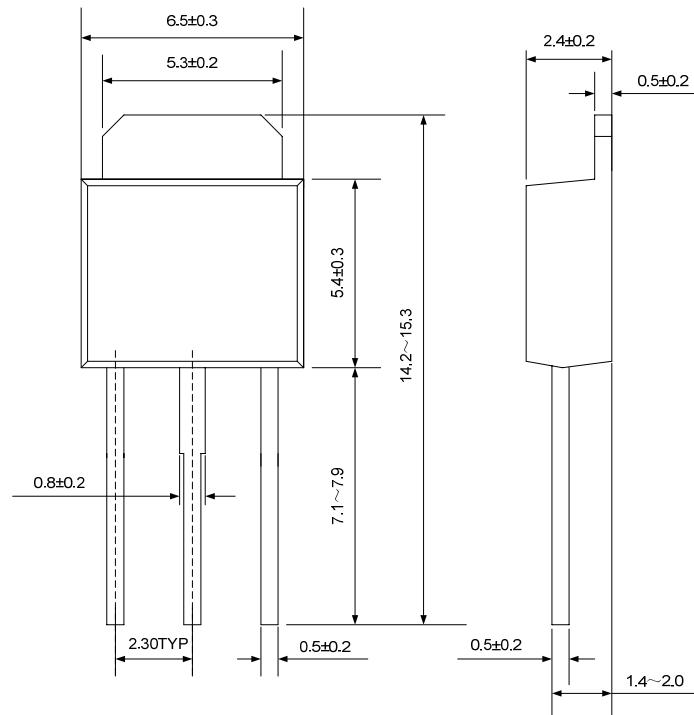
TO-220-3L

UNIT: mm



TO-251-3L

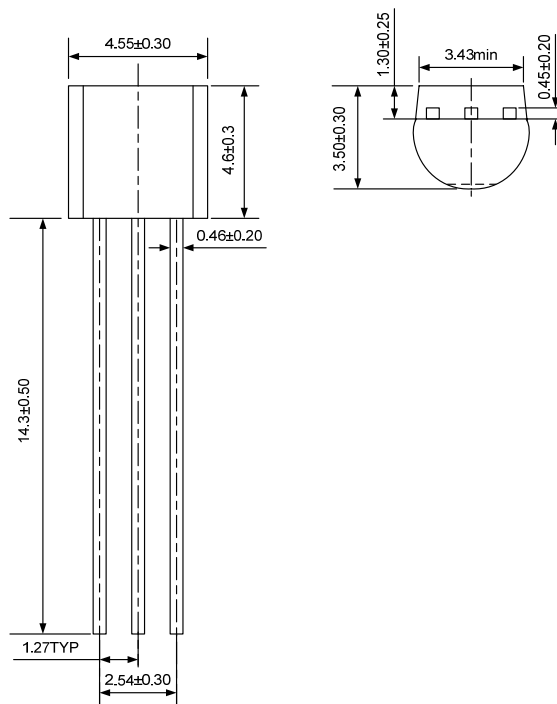
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PACKAGE OUTLINE(continued)

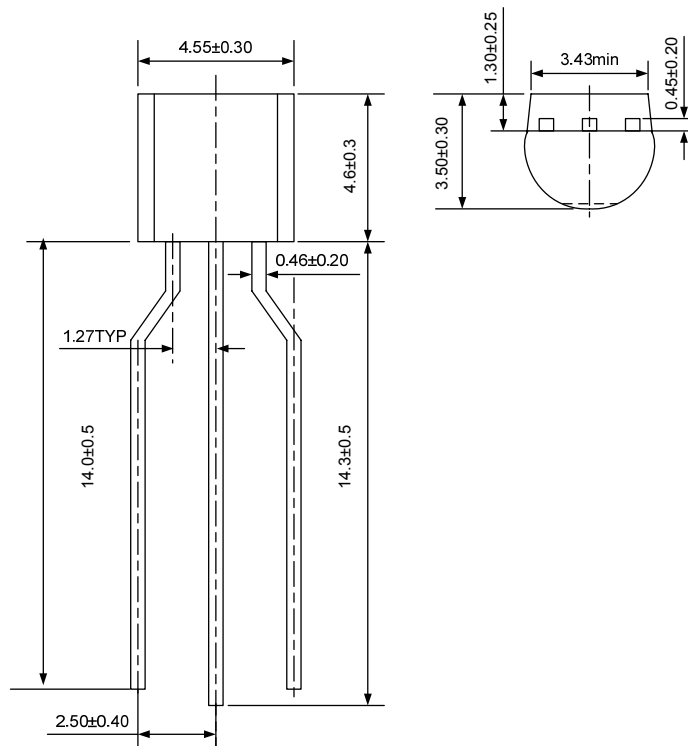
TO-92-3L(1)

UNIT: mm



TO-92-3L(2)

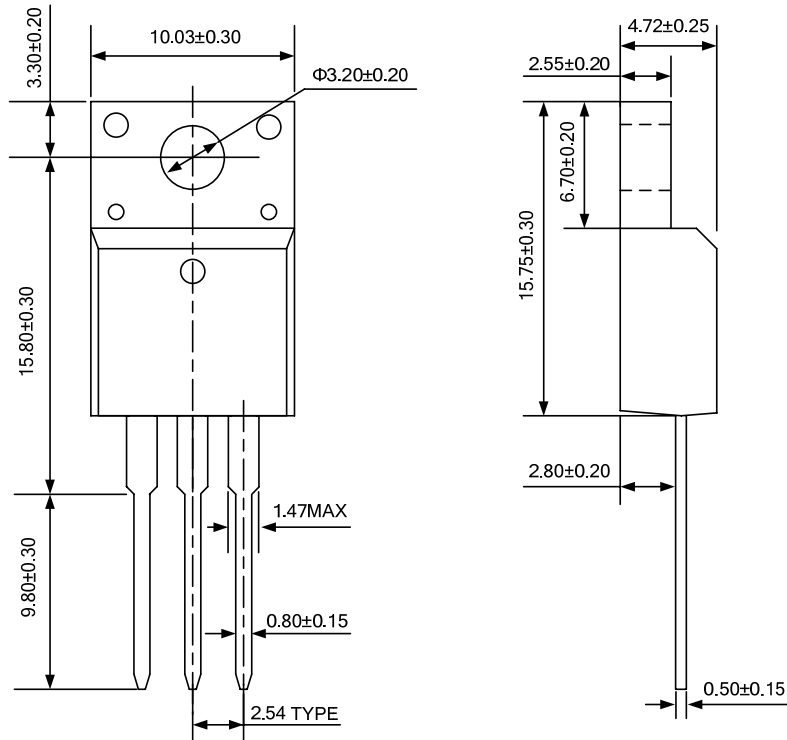
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PACKAGE OUTLINE(continued)

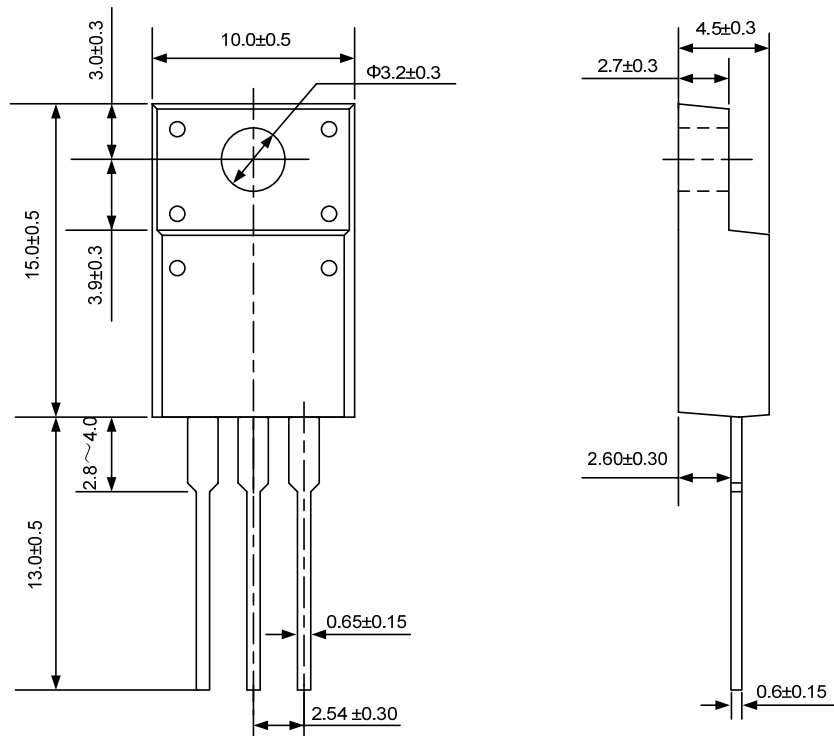
TO-220F-3L(1)

UNIT: mm



TO-220F-3L(2)

UNIT: mm



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- Silan will supply the best possible product for customers!

ATTACHMENT**Revision History**

Date	REV	Description	Page
2011.01.17	1.0	Original	